FlowCAD

FloWare
What's New

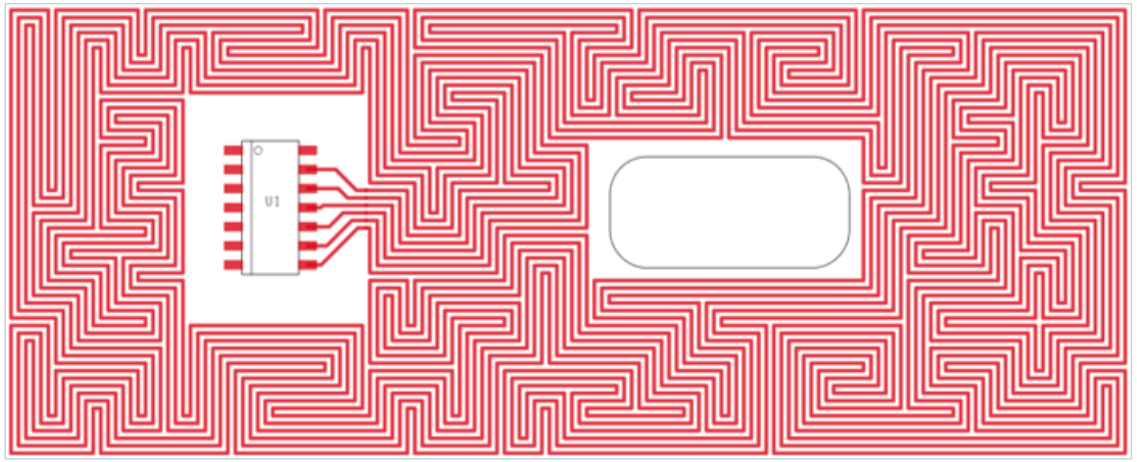
January 2023

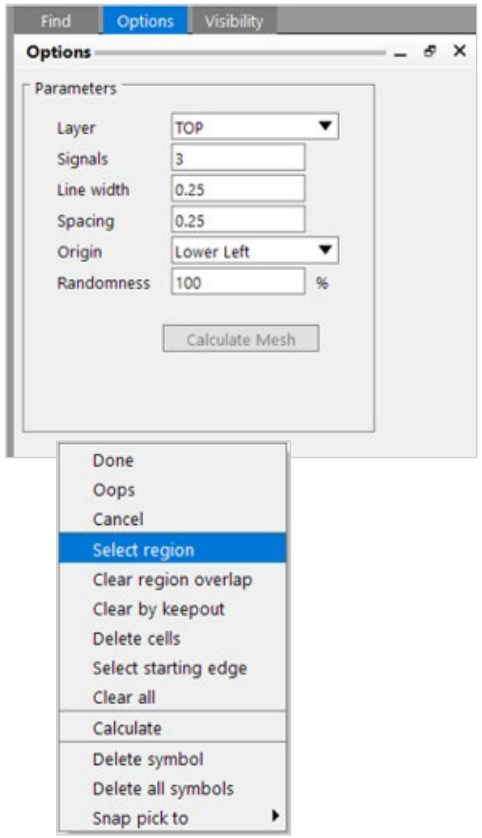
FloWare 2023 Q1

- Anti Tamper Mesh PCB
- Contour Place
- Digital Soldermask

Anti Tamper Mesh PCB

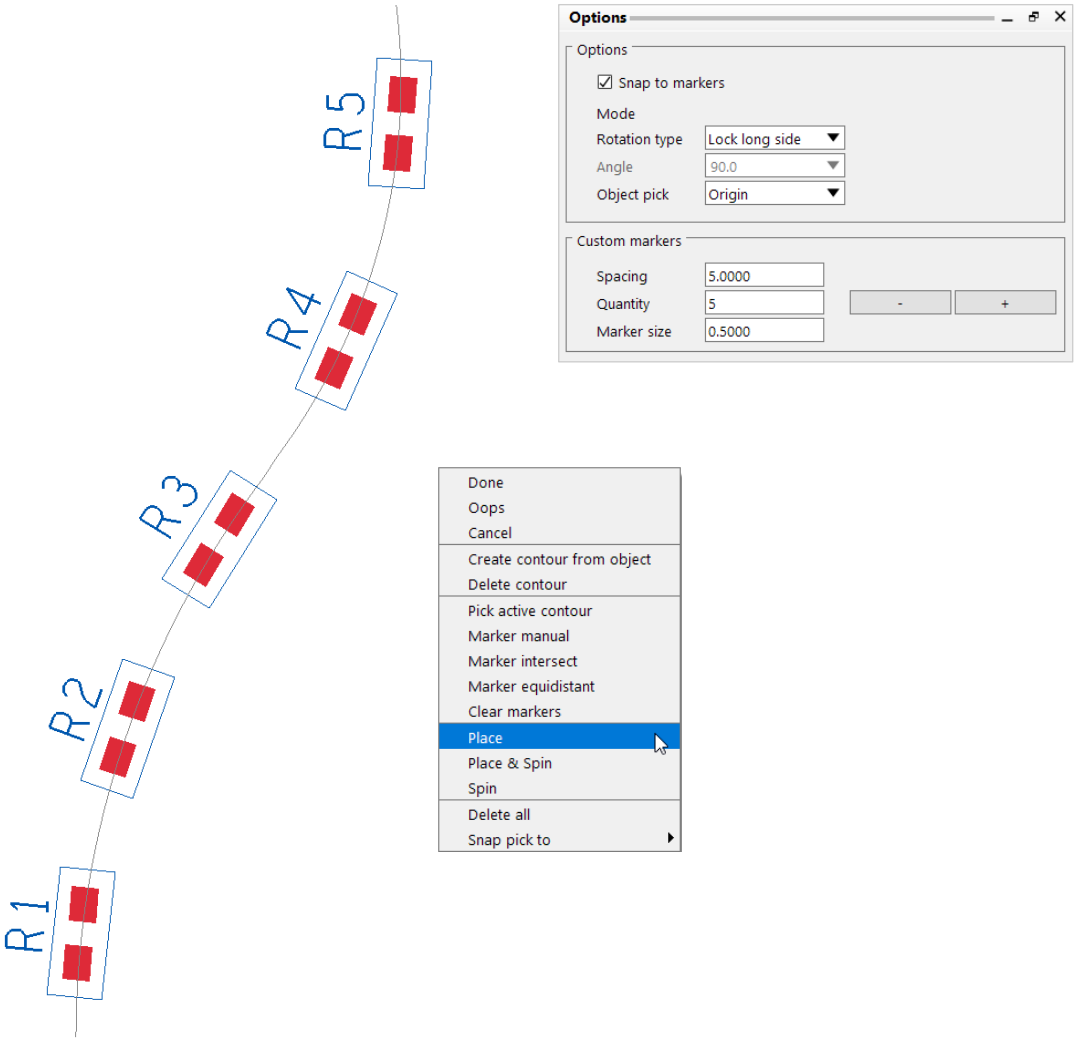
- Useful for Hardware Security Modules (HSM)
  - In order to actively detect and respond to external attacks a convoluted maze of wires (mesh) can be used to monitor changes in resistance, capacitance, breaks, shorts etc.
- Features
  - Number of signals, width, spacing, …
  - Region select, keepouts, destination layer, …
  - Randomness





Contour Place

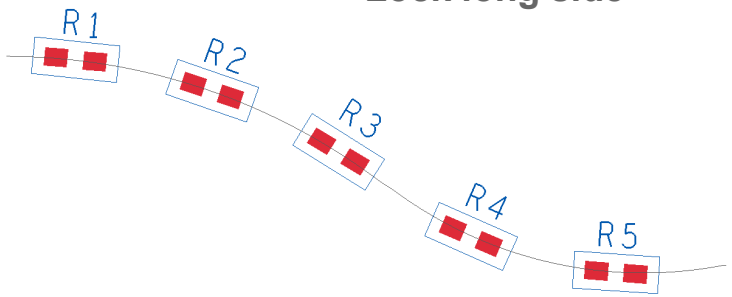
- Interactive placement along contour
  - Automatic snap to contour path
  - Place, Place & Spin, Spin
- Various alignment options
  - Lock long side
  - Lock short side
  - Relative
  - Absolute
- Custom snap marker
  - For accurate control
  - Manual markers
  - Markers by intersection
  - Equidistant markers

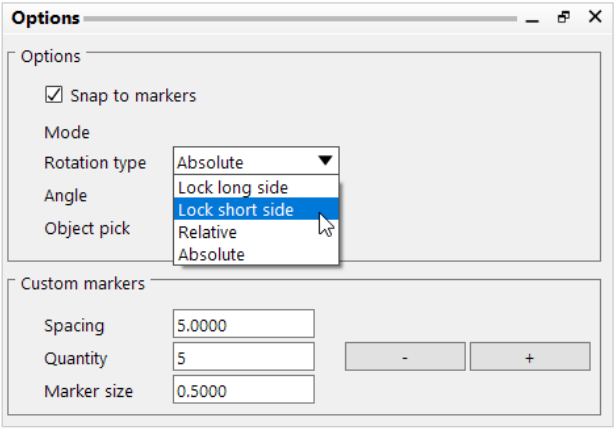


Contour Place

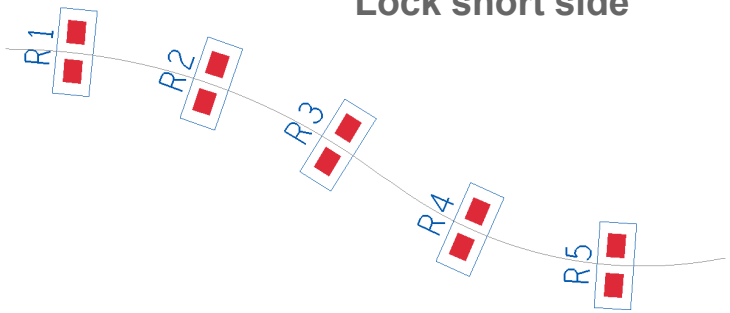
- Alignment options

Lock long side

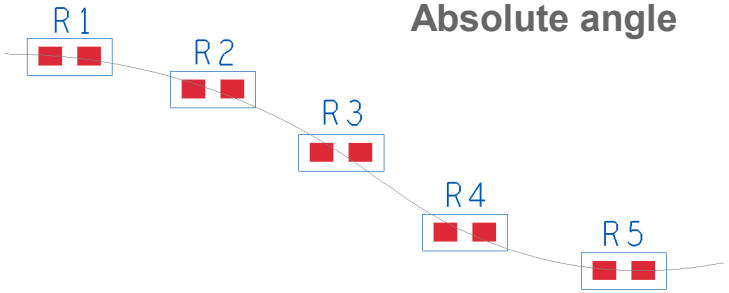




Lock short side

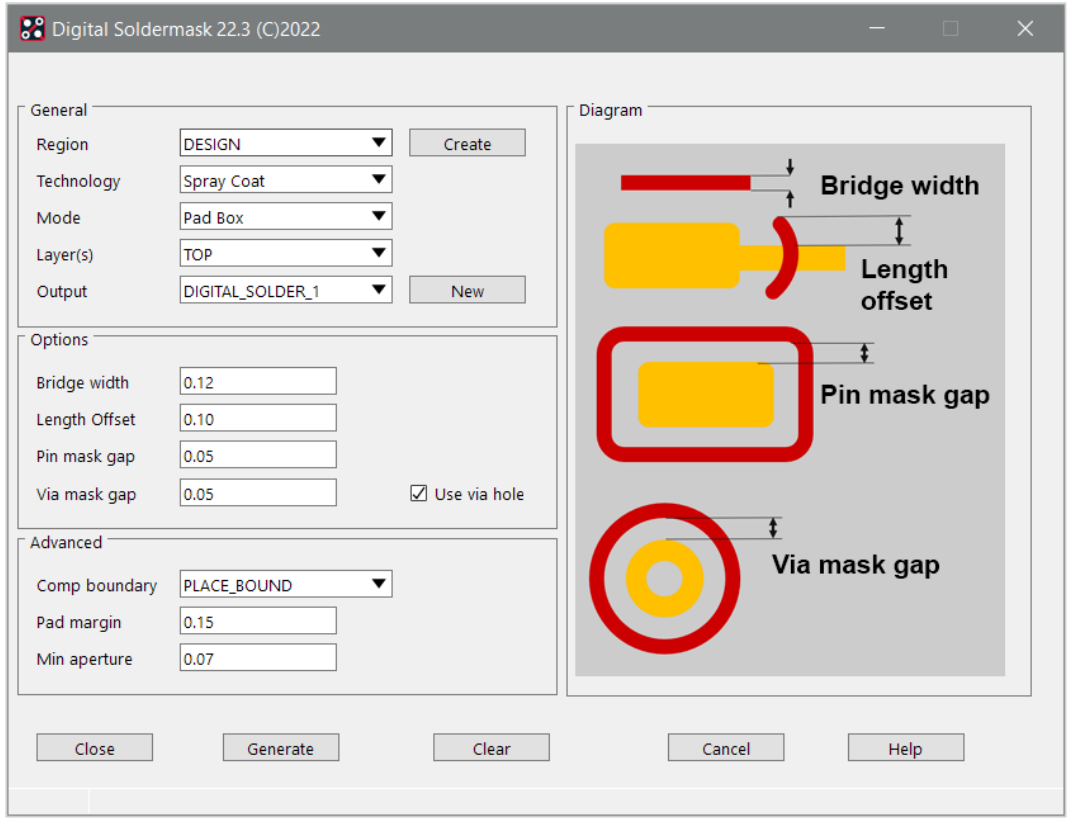


Absolute angle



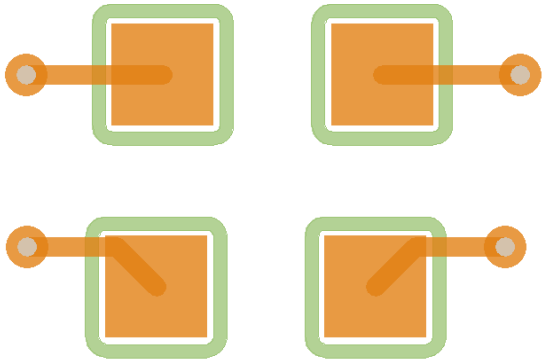
Digital Soldermask

- Additional features accounting for new technologies
- Developed together with Würth Elektronik
- Various modes
  - Pad ring / box
  - Trace mode
  - Component mode
  - By region
- Parameters
  - Bridge width
  - Pin, via gap
  - Length offset
  - …

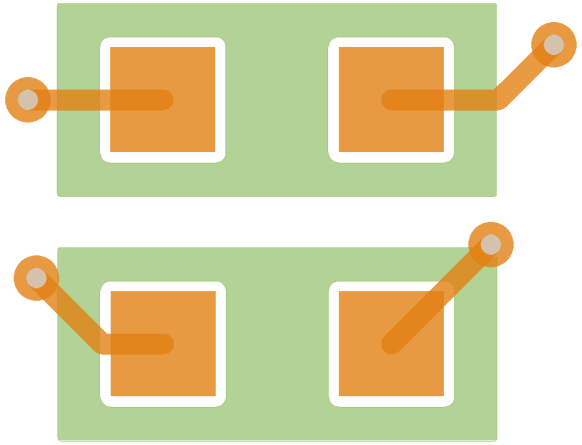


Digital Soldermask

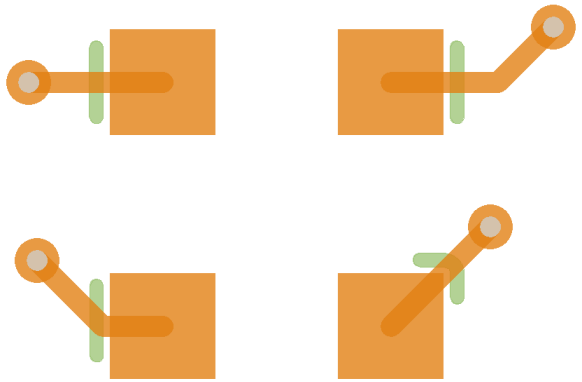
Pad box



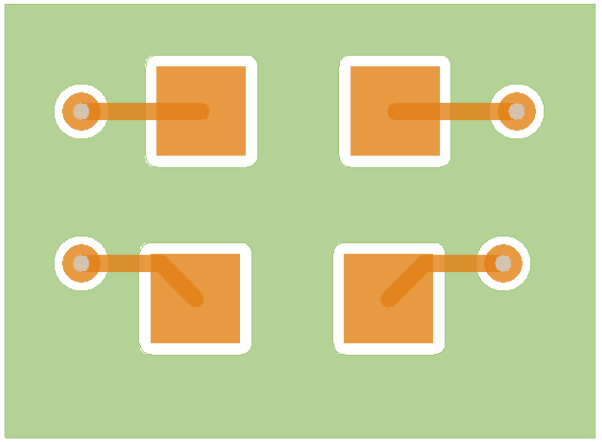
Component boundary



Trace mode



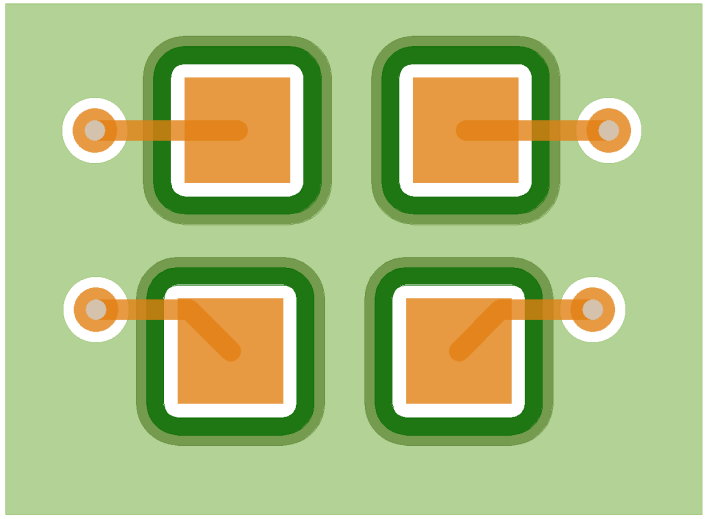
Soldermask region



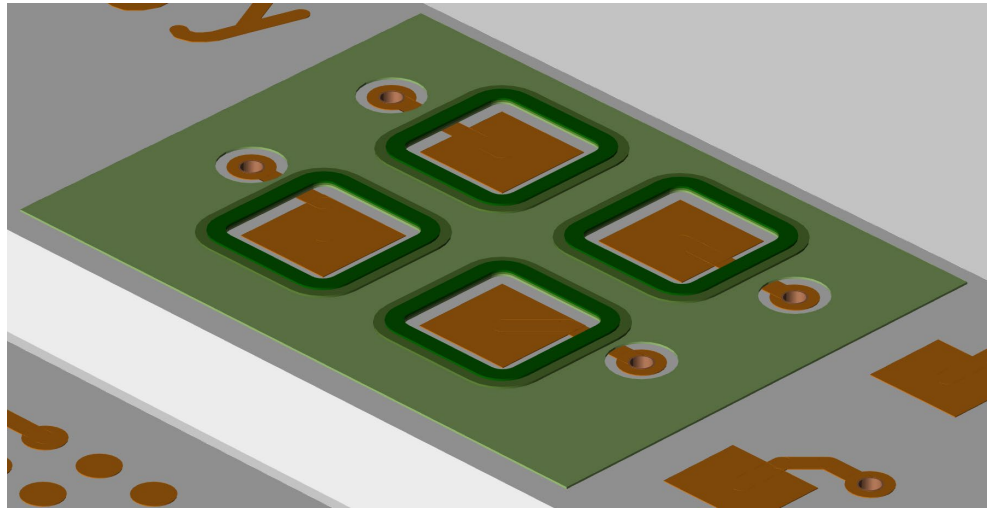
Digital Soldermask

- Techniques can be combined and used to create multiple masks on separate layers, accounting for mask thickness and thickness requirements

2D



3D canvas



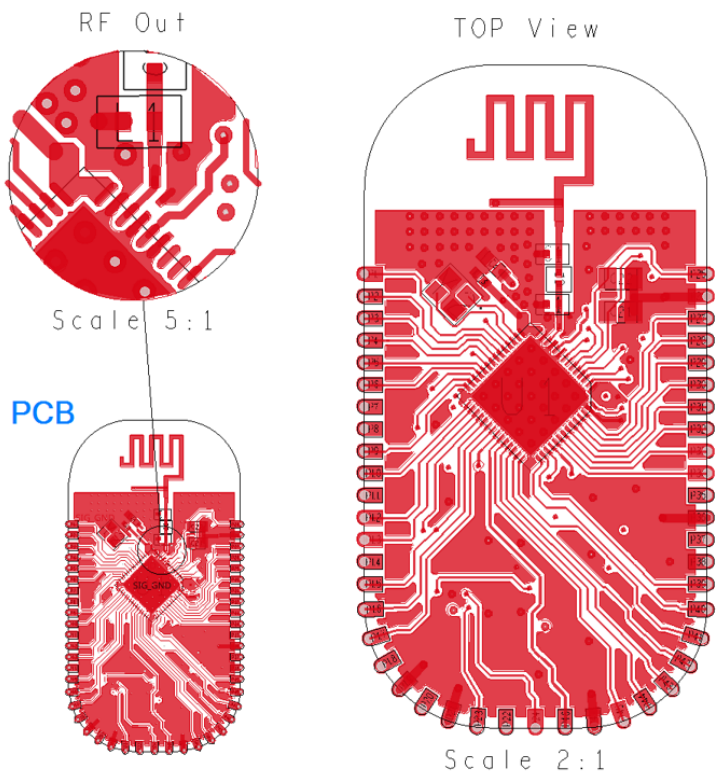
- In example above:
  - Solder mask region on Digital_Soldermask_1_TOP
  - Pad box on Digital_Soldermask_2_TOP
  - Pad box on Digital_Soldermask_3_TOP

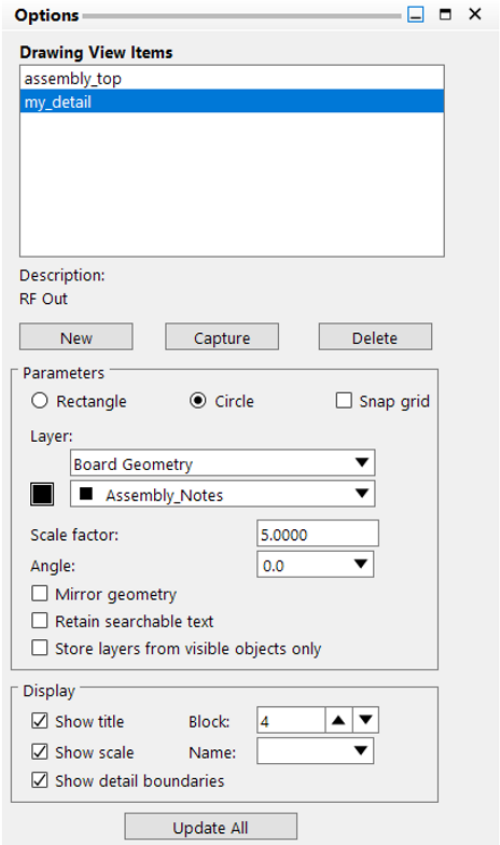
FloWare 2021 Q4

- Drawing View Manager

Drawing View Manager

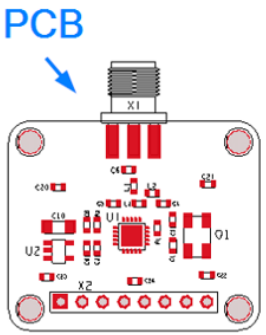
- Facilitates creation of manufacturing drawings
- Features
  - Capture named drawing view items interactively
  - Clipping capabilities using rectangular or circular boundaries
  - Scale, mirror, rotate
  - Retain object colors
  - Automatic update
  - Template support

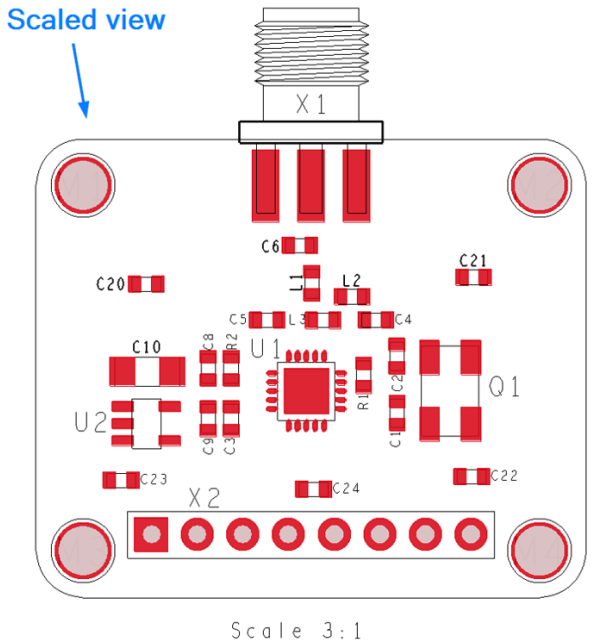


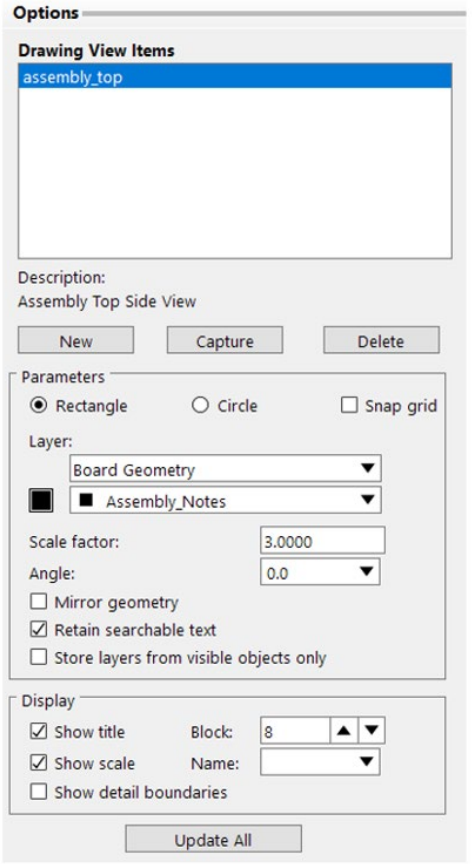


Drawing View Manager

- Simple use model
  - Press **New** and enter a name
  - Select item from the list
  - Press **Capture**
  - Adjust layer visibility and find filter…
  - Adjust mirror, scale, rotation…
  - Place item
  - Use **Update All** once PCB was modified

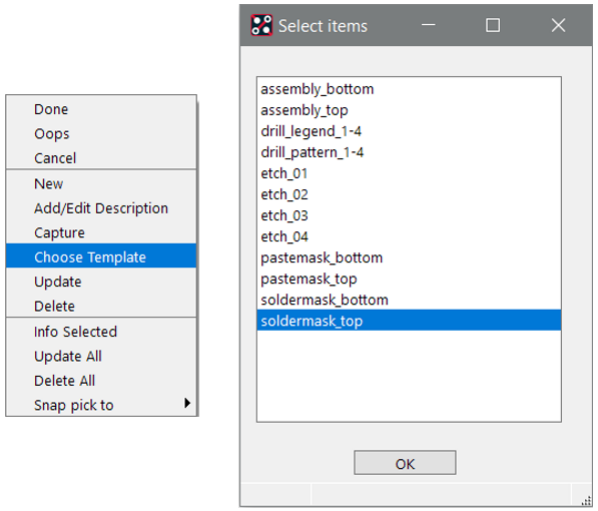


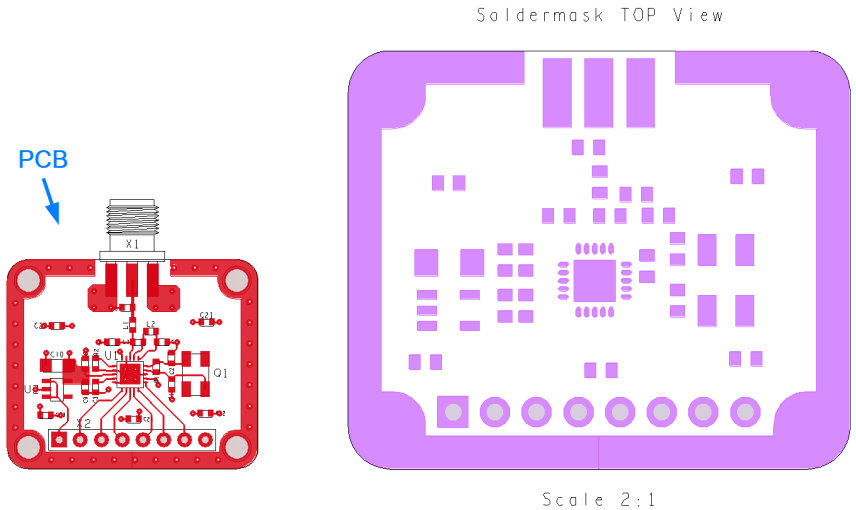




Drawing View Manager

- Template support
  - Significantly shortens setup time
  - Eliminates the need to create drawing view items each time from scratch in a new project
  - Information about visible layers, objects, source area, destination layer, scaling etc. is already pre-defined
  - Default templates located in **share/pcb/toolbox/config/drawingview**
  - SITE and pcbenv customizable
- Use model
  - **RMB – Choose Template** and select an item
  - If necessary adjust scale etc.
  - Place item



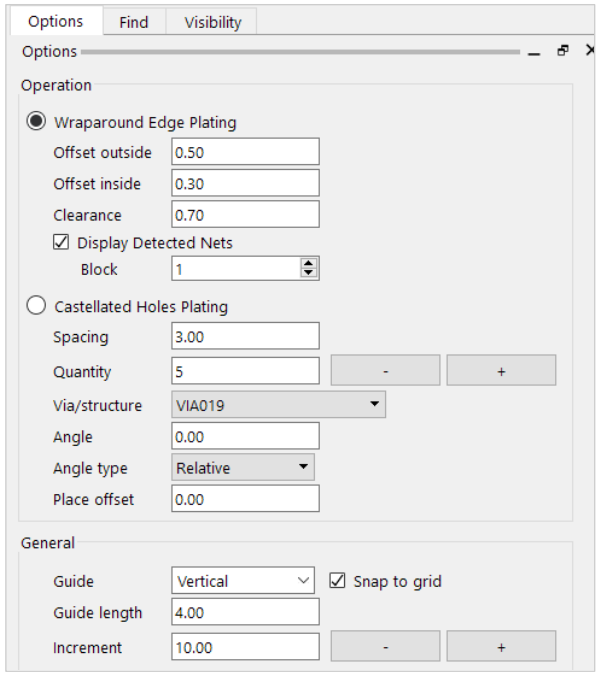


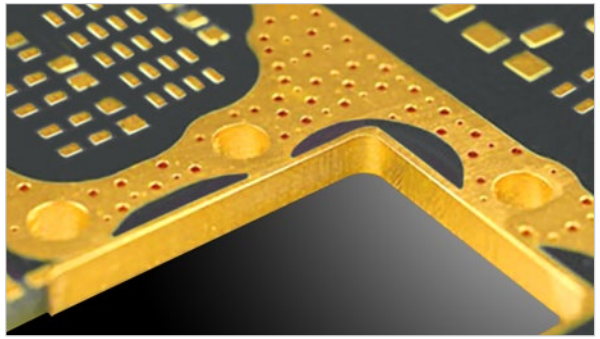
FloWare 2021 Q1

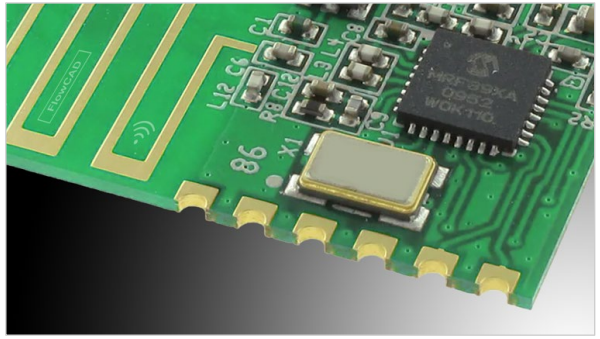
- Edge Plating
- Technical Cleanliness
- NC Panel Route

Edge Plating

- Edge plating is a plated conductive material on the edge of a PCB where in normal instances, only dielectric material is exposed
- This plated conductive material may be used for many functions
  - Improve current carrying across multiple layer of a PCB
  - Edge connection protection
  - Board to case grounding
  - EMC signal integrity
  - Heat management
- Two forms of Edge Plating
  - Wraparound (Side) Plating
  - Castellated Holes

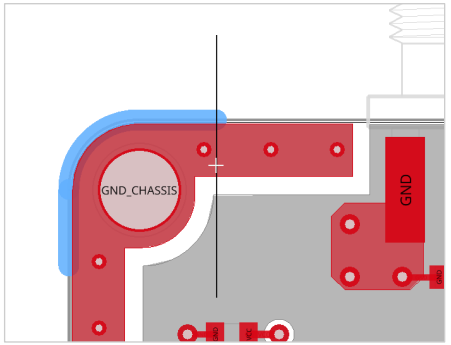


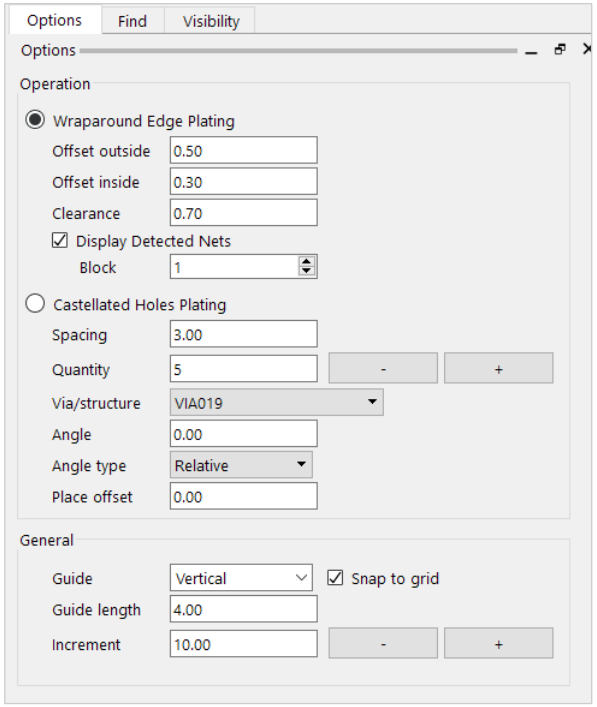


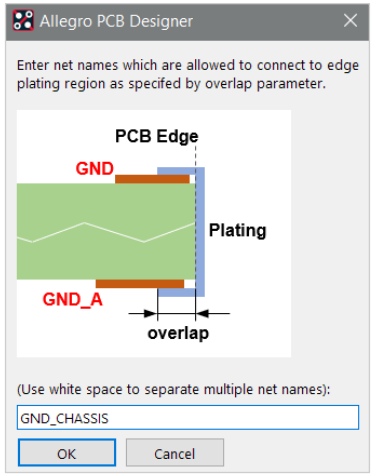


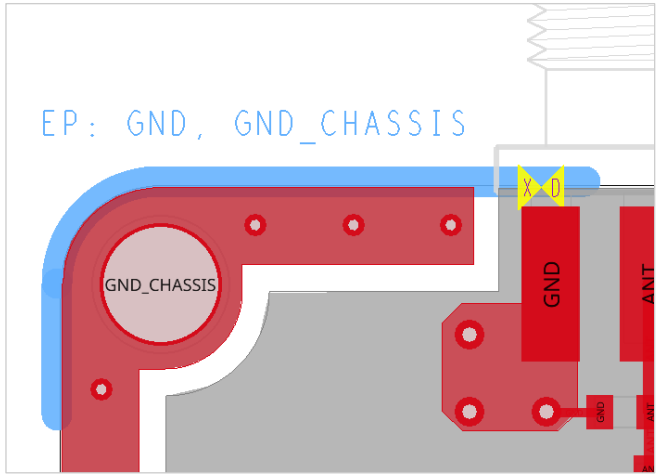
Edge Plating: Wraparound (Side)

- Define plating sections interactively
- Net assignment
- Connectivity Check
- DRC Clearance Check
- Net Short support



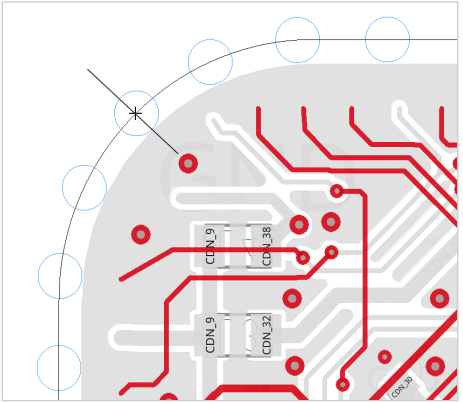


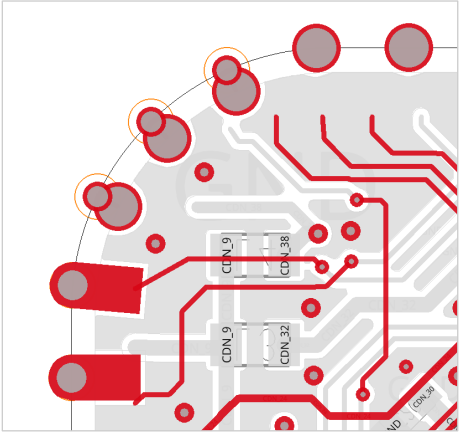


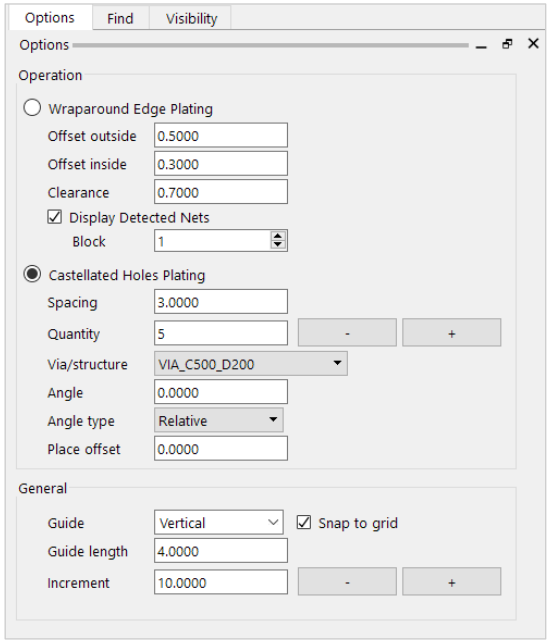


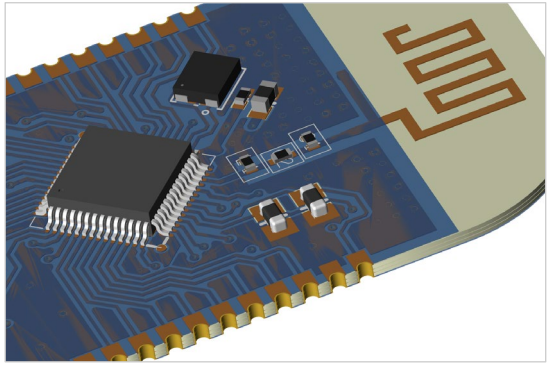
Edge Plating: Castellated Holes

- Define locations interactively along outline supporting
  - Spacing
  - Quantity
- Objects supported
  - Vias
  - Via structures
  - Symbols
  - Electrical components
- Placement parameters
  - Alignment with outline (relative, absolute)
  - Offset from outline



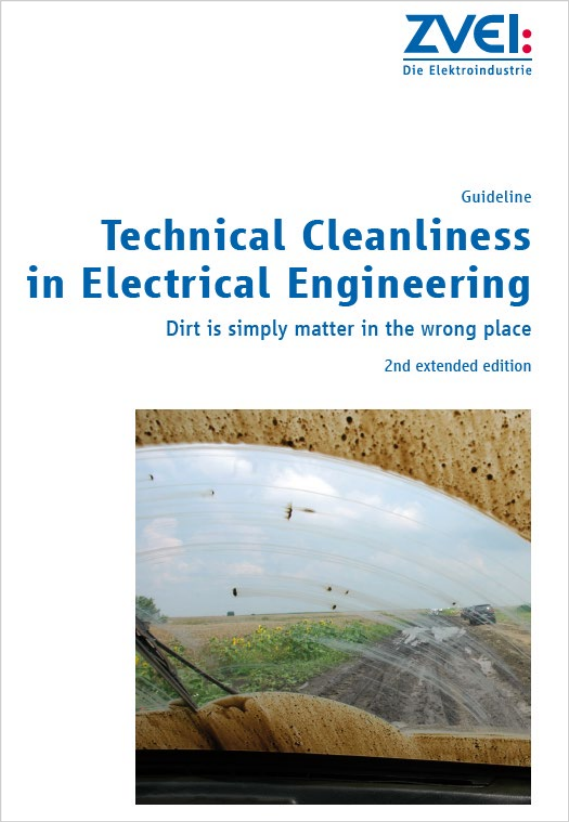






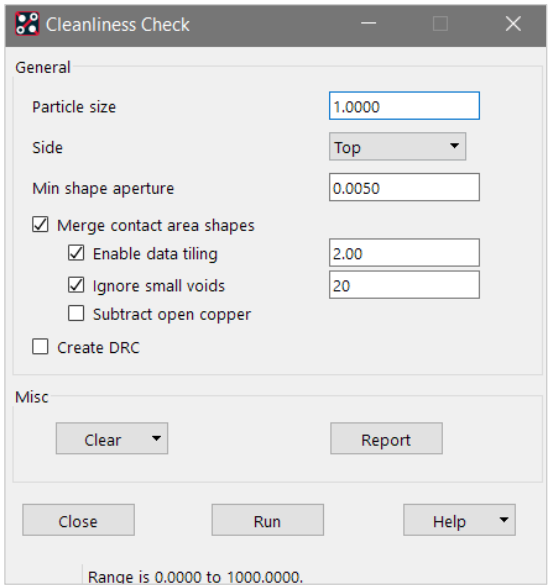
Technical Cleanliness

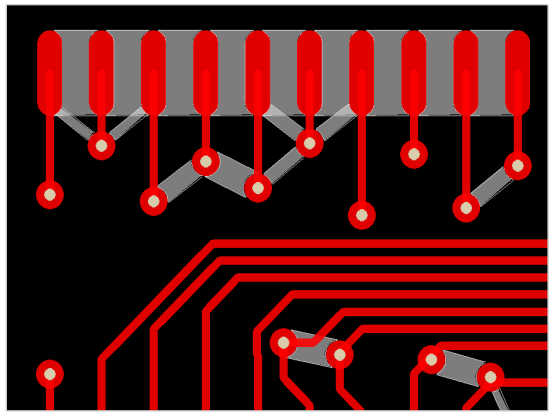
- Technical Cleanliness refers to the performance of components, assemblies and systems related to particle contamination in automotive and other applications
- On PCB's such particles (e.g. conductive particle from aluminum cover) may cause short circuits
- The probability failure depends on
  - Particle size
  - Contact area size
  - Number of contact areas
- For more information refer to document ZVEI Guideline for Technical Cleanliness from https://www.zvei.org/



Technical Cleanliness

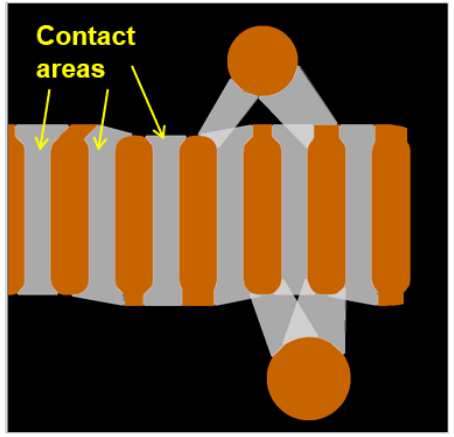
- Analyzes the PCB layout for contact areas caused by particles with a given size
- The contact area specifies the area in which a particle will cause a short, no matter how the particle is oriented
- Cleanliness Check calculates and visualizes contact areas using shapes and writes a report
- By sweeping the particle size the information from the output can be used to feed cleanliness assessment calculator from ZVEI

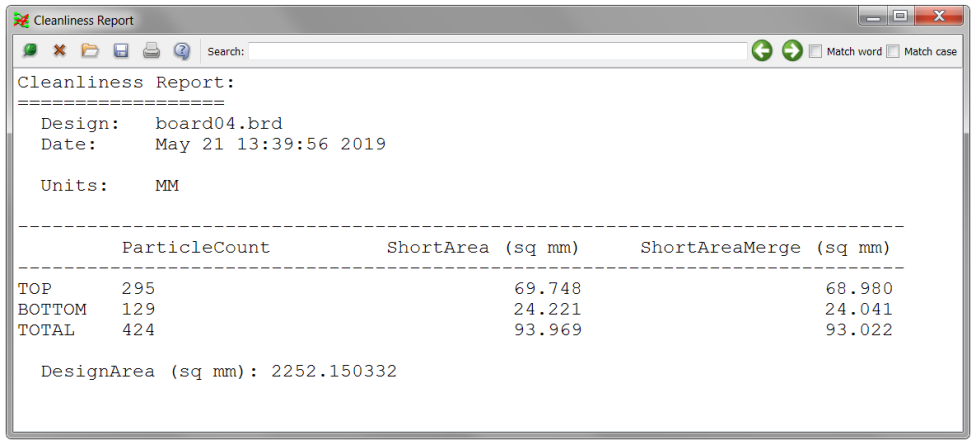




Technical Cleanliness

- Menu button Report
- Particle count per layer
- Short Area
  - Sum of particle shape areas from layer **CLNS_CONTACT_TOP (BOTTOM)**
- Short Area
  - Shape area on merged layer **CLNS_RESULT_TOP (BOTTOM)**
- Design Area
  - Area from **DESIGN_OUTLINE** minus **CUTOUT**



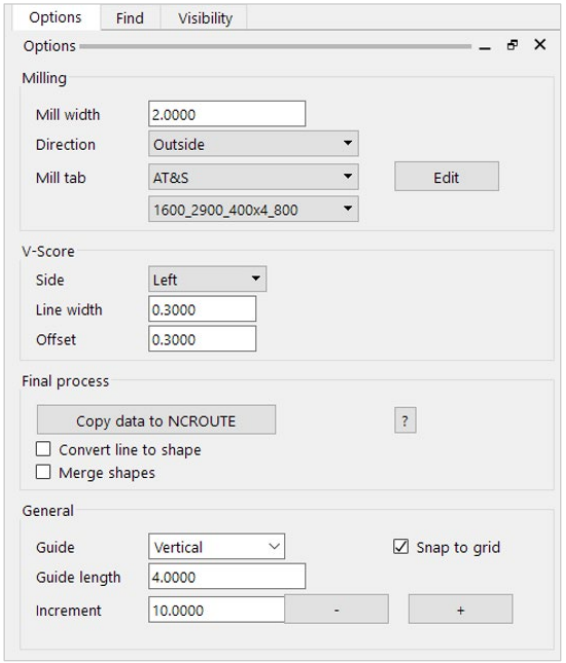


Cleanliness Report

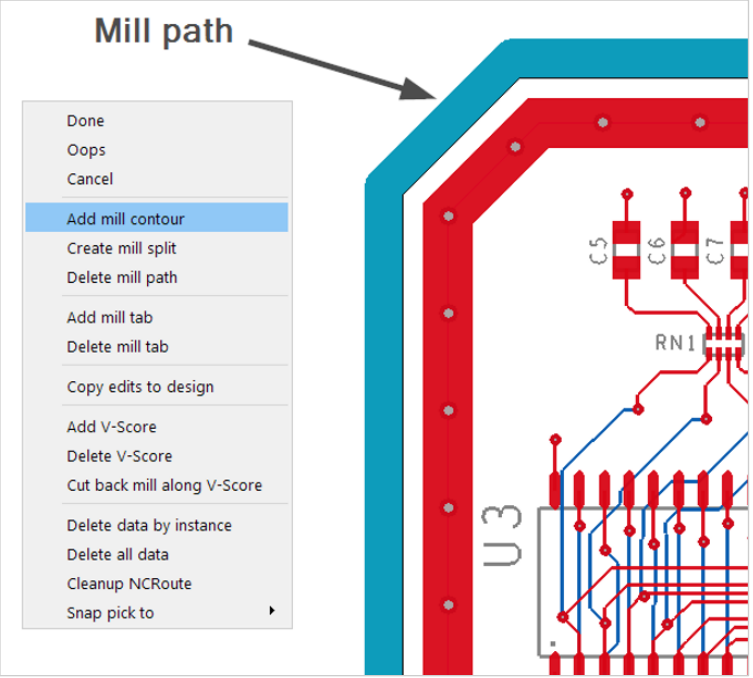
```
Cleanliness Report:
===================
  Design:    board04.brd
  Date:      May 21 13:39:56 2019

  Units:     MM

-------------------------------------------------------------------------------
          ParticleCount          ShortArea (sq mm)      ShortAreaMerge (sq mm)
-------------------------------------------------------------------------------
TOP       295                                69.748                     68.980
BOTTOM    129                                24.221                     24.041
TOTAL     424                                93.969                     93.022

  DesignArea (sq mm): 2252.150332
```

NC Panel Route

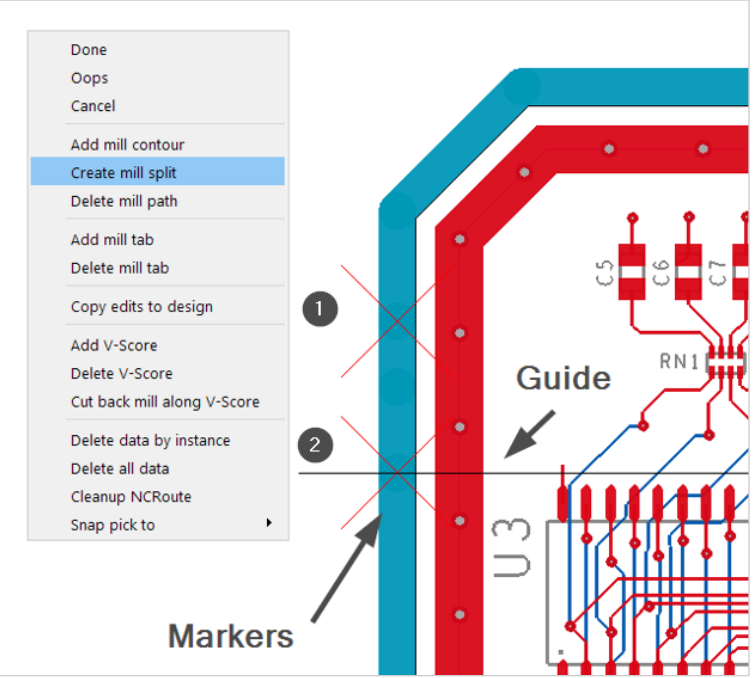
- Toolset supporting various techniques for PCBs in a panel to be easily separated after their are manufactured and assembled
- Mill tab panels
  - Add mill contour
  - Split & Cut mill
  - Add mill tabs with or without perforation drills
- V-Score panels



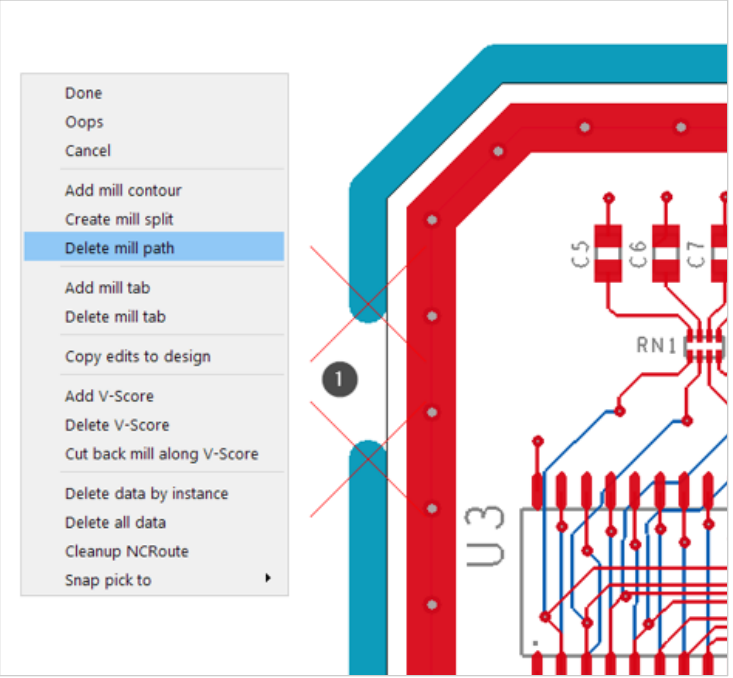
NC Panel Route



Add mill contour along the edge of the board



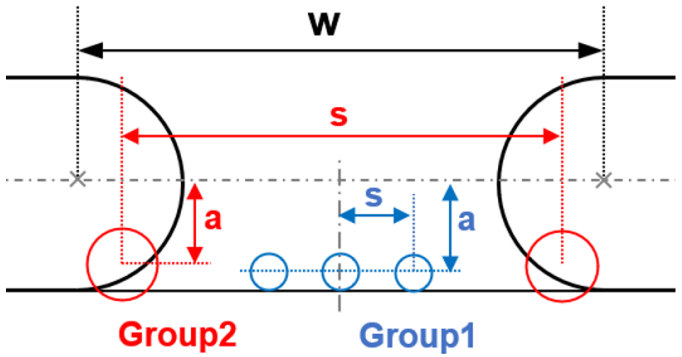
Create splits interactively

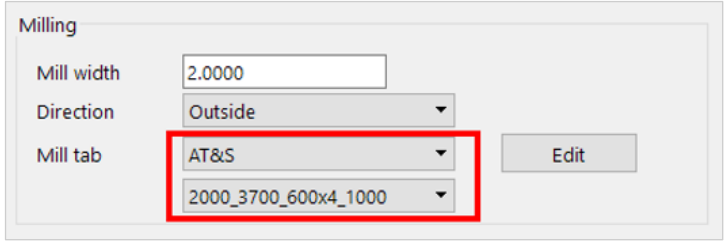


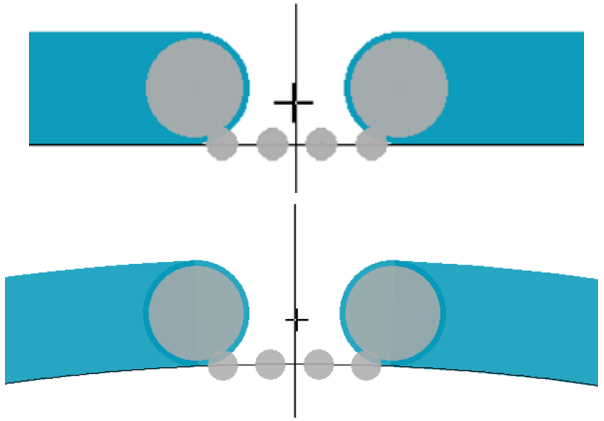
Delete splits

NC Panel Route

- Mill tabs can be specified with respect to
  - Tab size
  - Number of holes, diameter spacing and offset
- Application provides libraries from PCB fabricators
  - AT&S
  - Fineline
  - Alba PCB Group / Q-print electronic
- Interactive placement
  - Can be placed on any contour





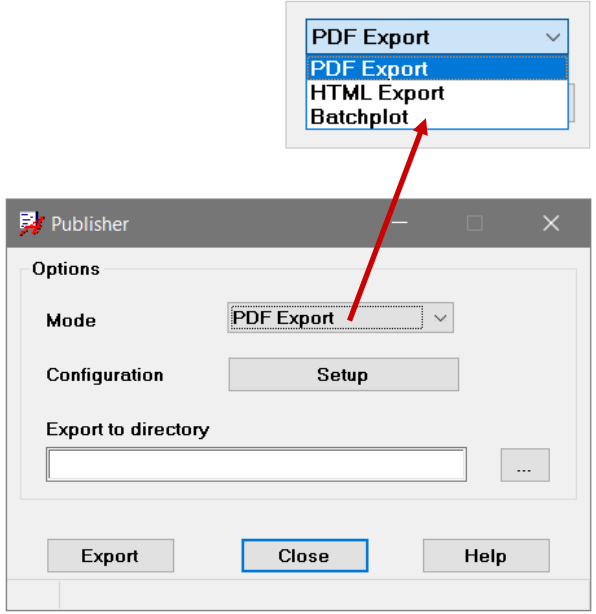


FloWare 2020 Q2

- **Batchplot Automation**
  - Overhaul
  - Now supporting native PDF Export from OrCAD / Allegro
- **Cross Section Generator**
  - Overhaul
  - Enhanced support for Rigid-Flex
- **Padstack Finder**
  - Support for Stacked Vias navigation
- **FloWare Installer**
  - Simplification of installation process
  - Consistency checks

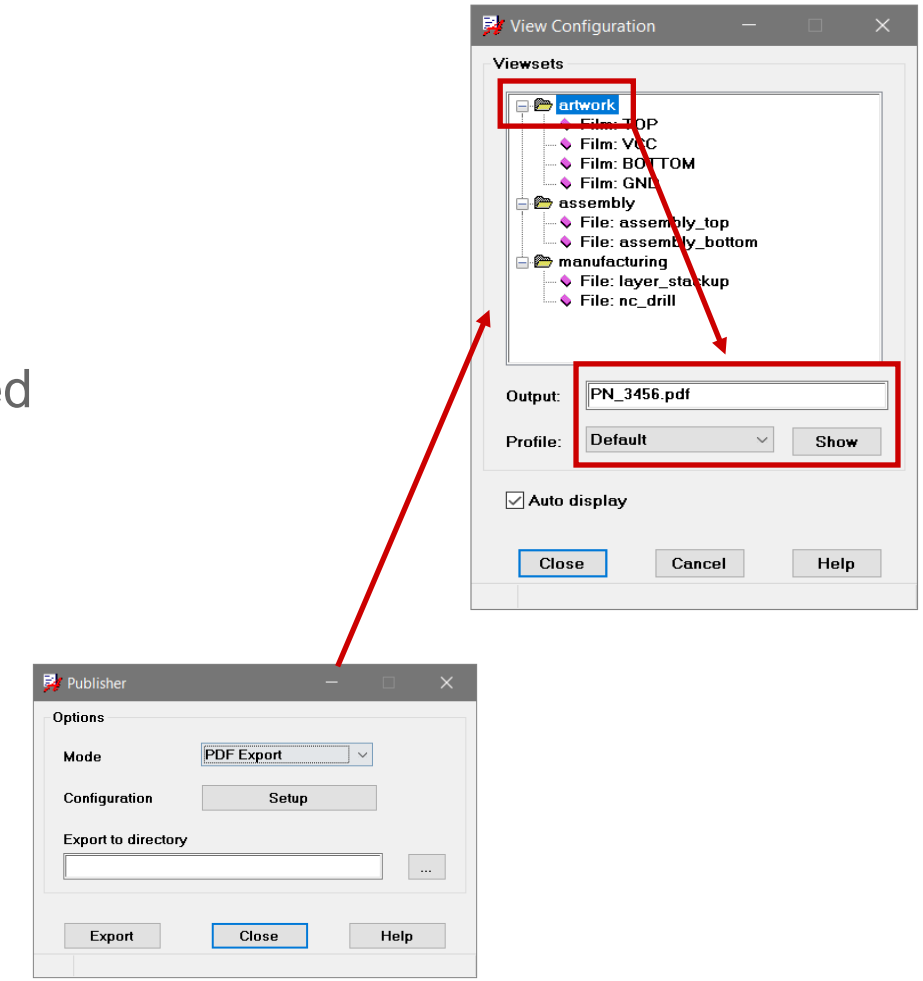
Batchplot Automation

- Now integrating PDF Export from Allegro / OrCAD PCB Editor
- Three modes
  - PDF Export
  - HTML Export
  - Batchplot (legacy)



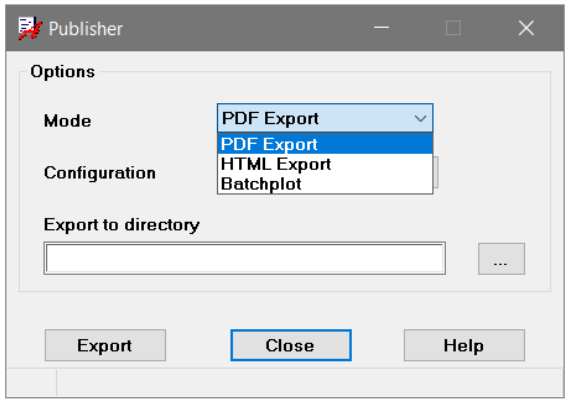
Batchplot Automation

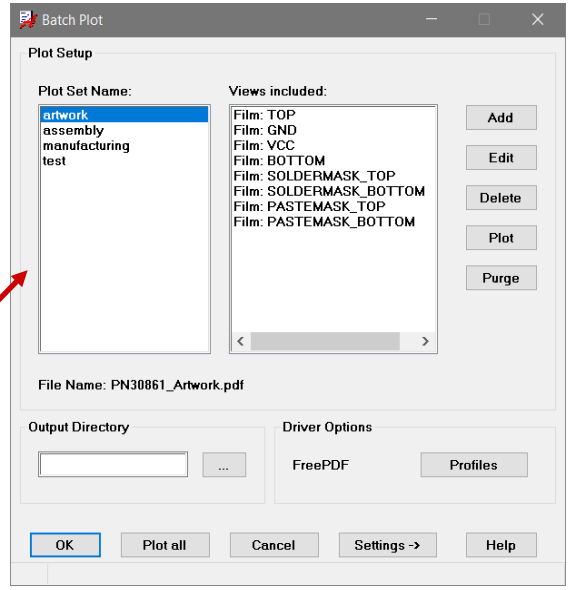
- Multiples viewsets can be defined
- A viewset may contain
  - Film records
  - Color views(!!)
- Each viewset corresponds to one PDF file to be generated
  - Name of the PDF file can be specified (output)
- Each viewset may reference a profile to be used during PDF export
  - E.g. black white print only
  - With / without meta data
  - …
- Single push button to generate all data ...



Batchplot Automation: Other Modes

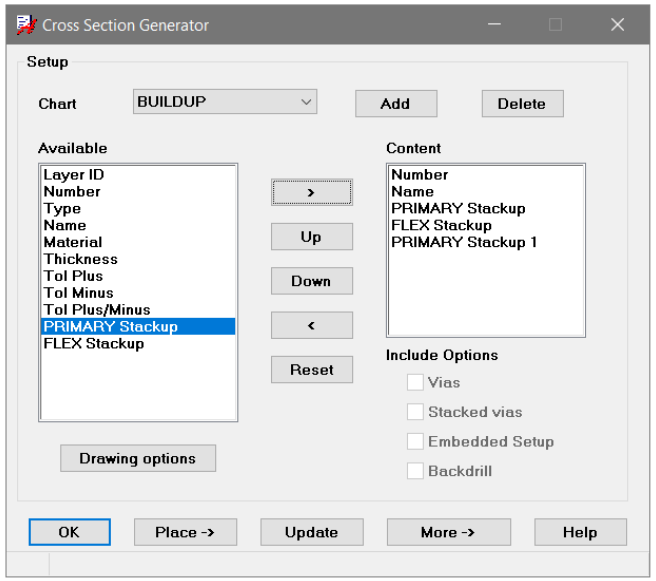
- **HTML Export**
  - Generates an HTML report including SVG graphics
  - Setup regarding viewsets and profiles similar to PDF Export
- **Batchplot (legacy)**
  - Selecting **Setup** will launch the existing / legacy application
  - Still available and supported

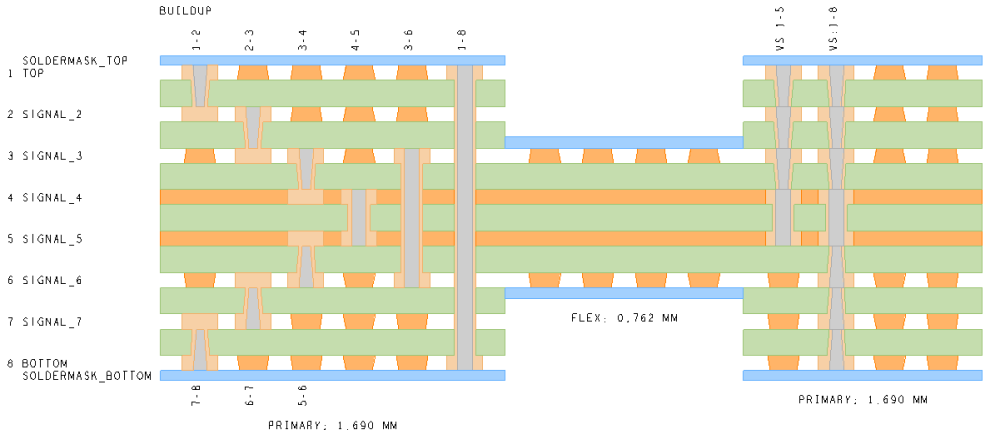




Cross Section Generator

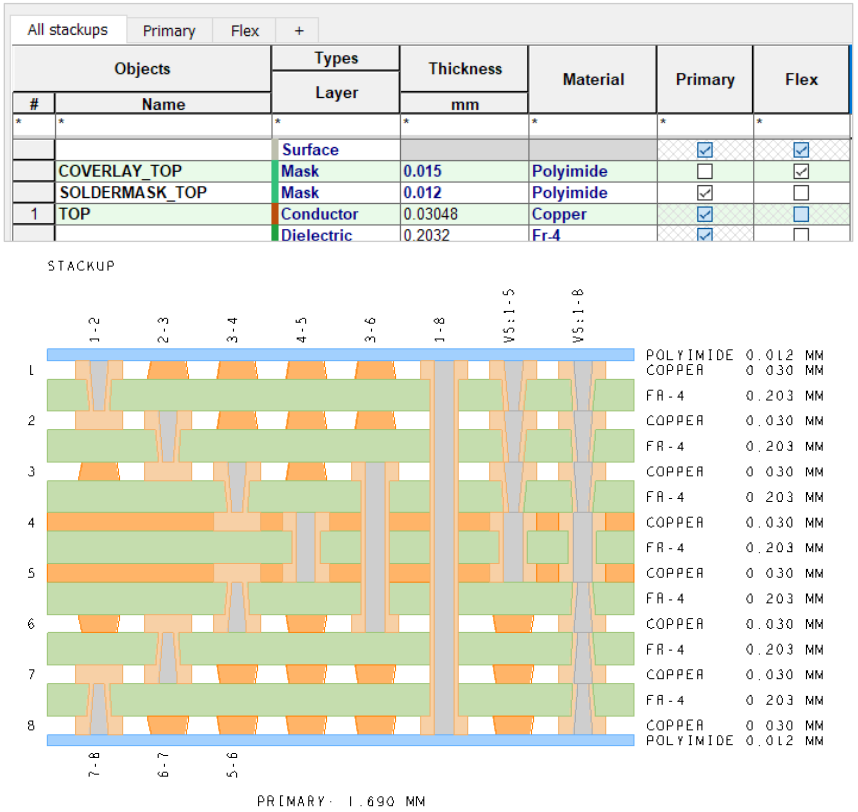
- Enhanced support for rigid-flex applications
- Customizable content
  - Custom charts with more meaningful visualization
  - Layer attributes, order, …
  - Colors, fill styles, …
  - Vias, stacked vias, backdrill and embedded status support
- SVG export
  - Export graphics for documentation purposes
- Configuration stored in db
- Automatic update

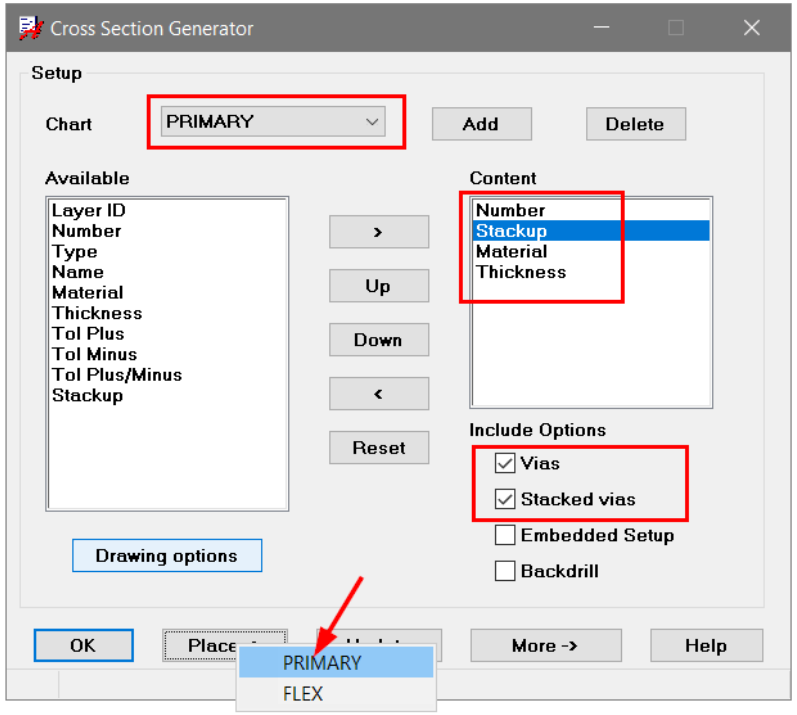




Cross Section Generator

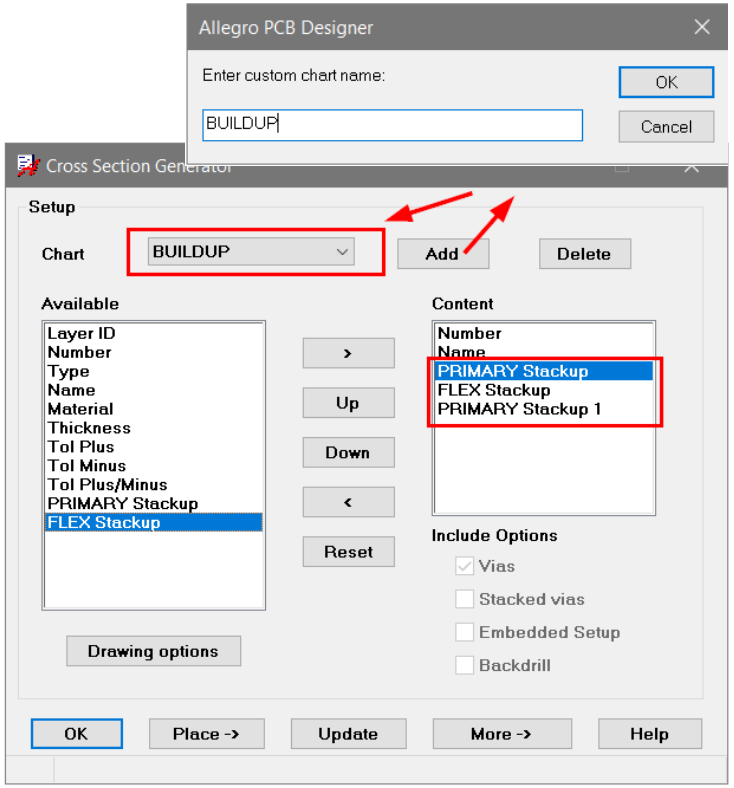
- Content can be defined for each stackup from cross section individually
- Also symbols can be placed individually

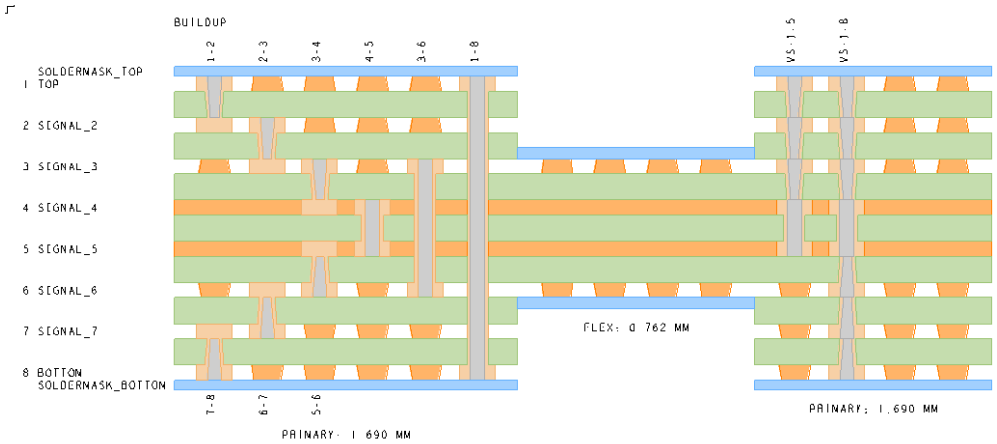




Cross Section Generator

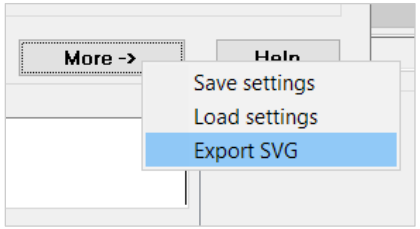
- A custom chart let's you combine stackups in an arbitrary order
- Feature many customer were asking for ...
- Additional information (vias, stacked vias, etc., can be applied to each stackup item individually)

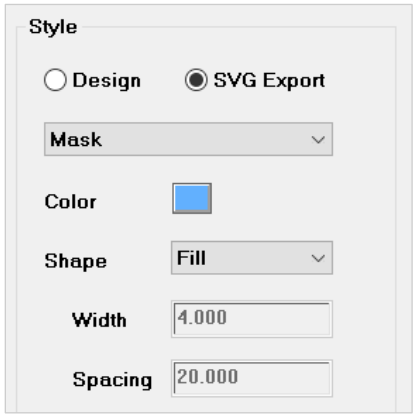


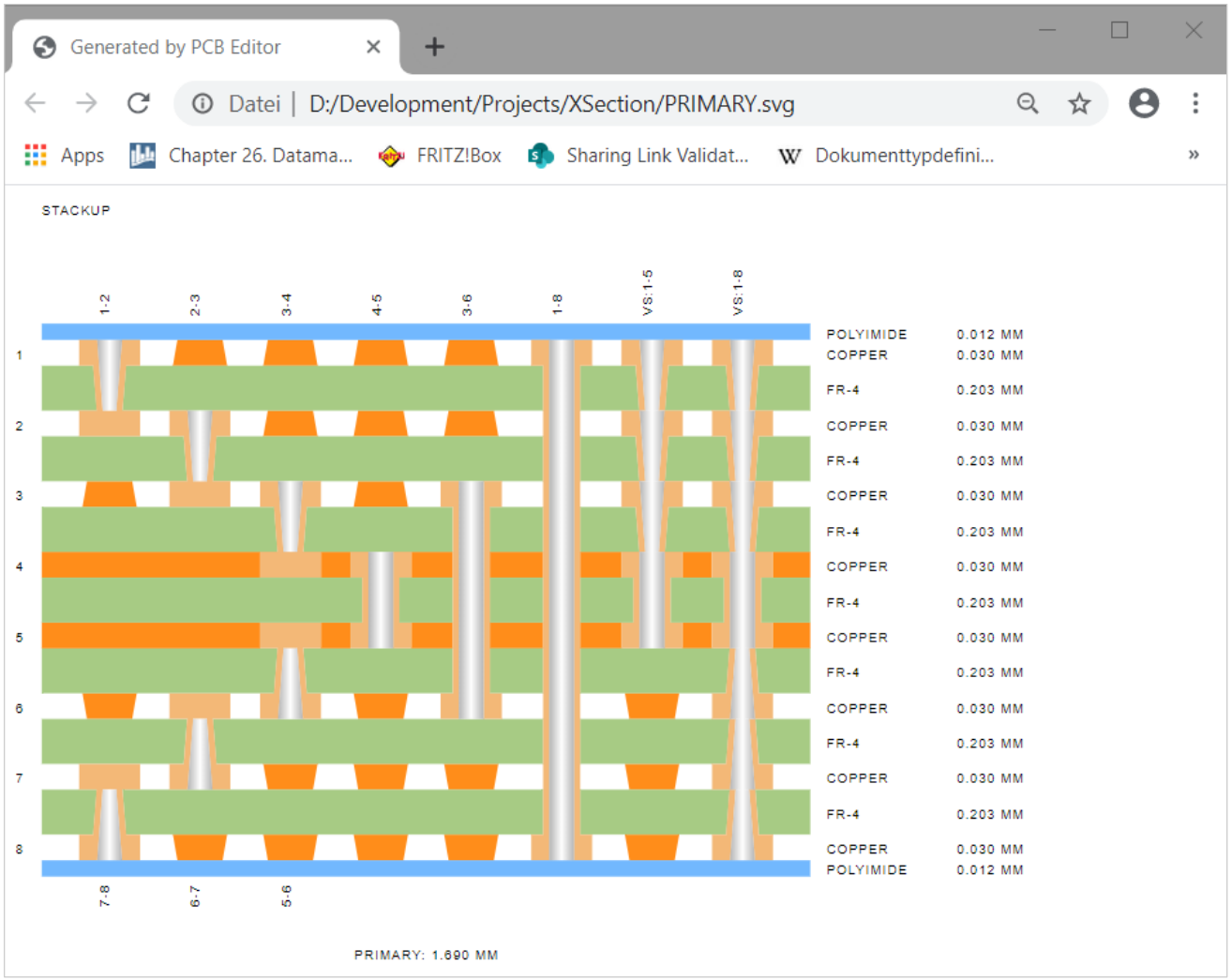


Cross Section Generator

- Export SVG
  - Mainly for documentation purposes
  - Separate color profile can be defined

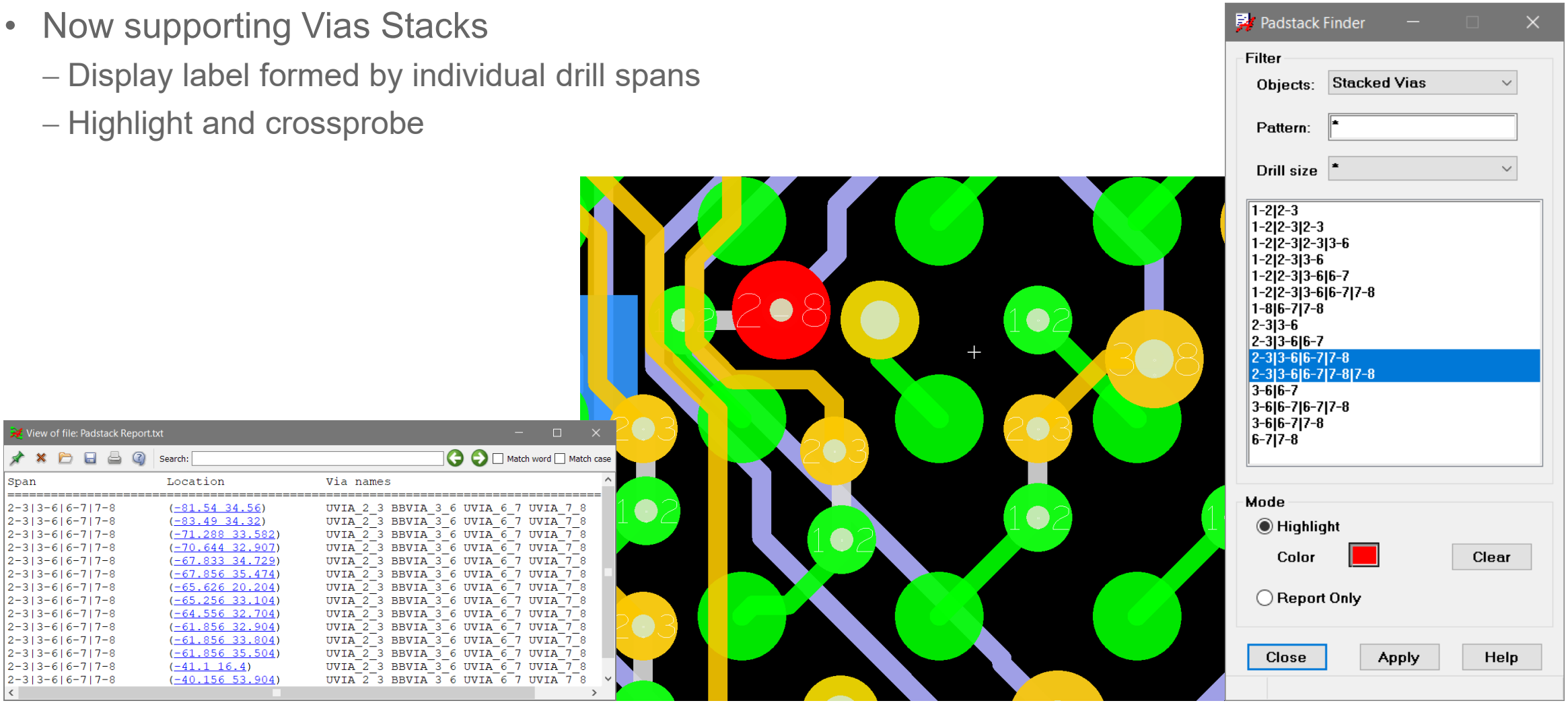






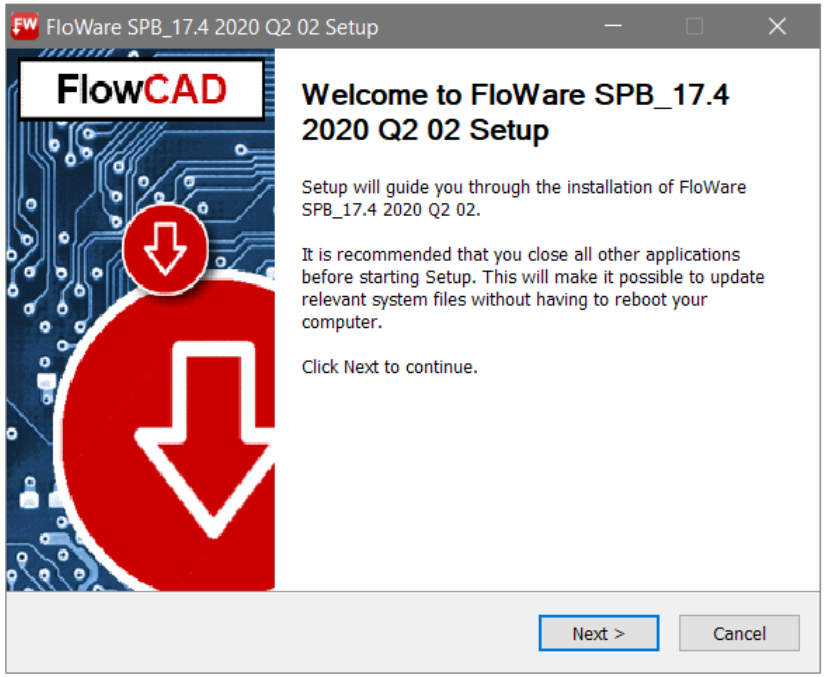
Padstack Finder

- Now supporting Vias Stacks
  - Display label formed by individual drill spans
  - Highlight and crossprobe



FloWare Installer

- **Simplification of installation process**
  - For consistency reasons FloWare stream will be always installed into installation tree share\pcb\etc
- **Additional consistency checks**
  - Duplicate installations in site and user environment
  - Status of license file

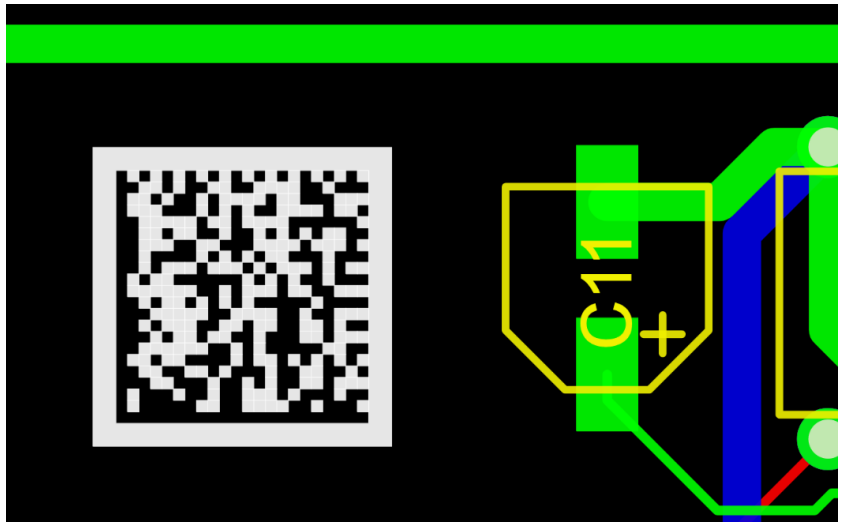


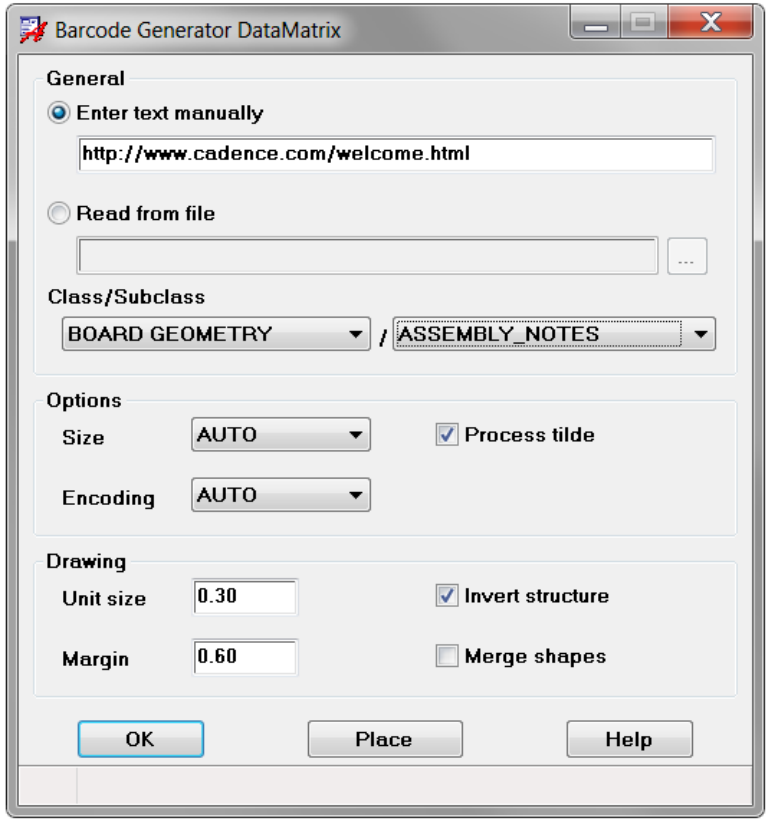
FloWare 2019 Q1

- **Barcode Generator**
  - Now supporting Data Matrix in addition to Code 39, Code 128 and QR Code
- **Fixes / Enhancements**
  - Advanced Testpoint Check
  - AOI Check
  - Quick Symbol Edit

Barcode Generator Support for Data Matrix

- De facto standard for product identification, tracking and other data-driven applications in the industry



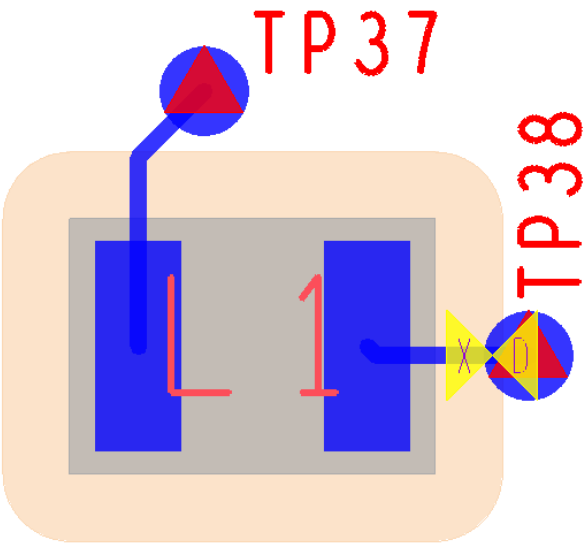


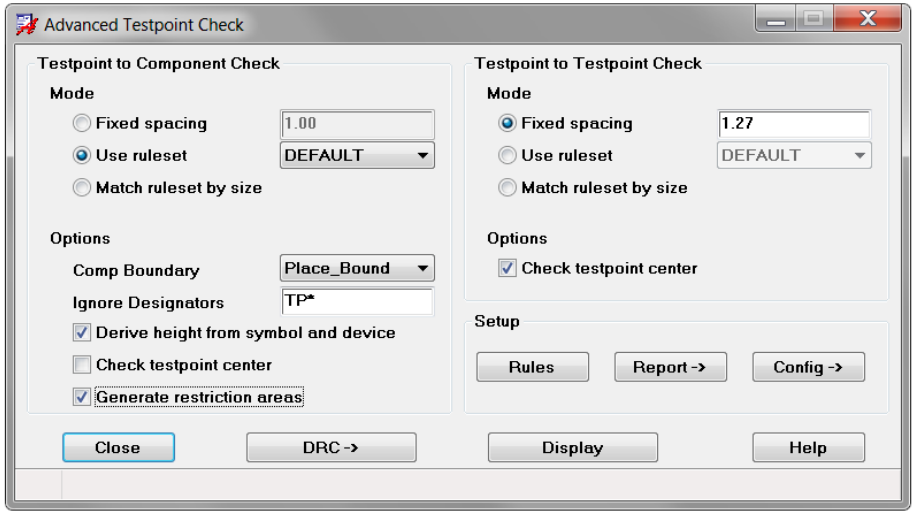
FloWare 2018

- **New modules**
  - Advanced Testpoint Check
  - AOI Check
  - SVG Export
- **Fixes / Enhancements**
  - Design Compare
  - Shield Router
  - ZDRC
  - Panelization

Advanced Testpoint Check

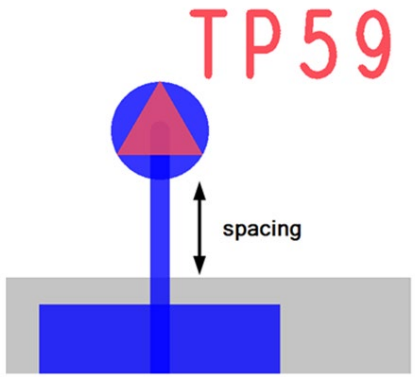
- Addresses various rules for testpoint checking
  - Testpoint to Testpoint check
  - Testpoint to Component check taking component height into account
  - Visualization of restriction areas
  - DRC marker generation
  - Constraints reuse through configuration files

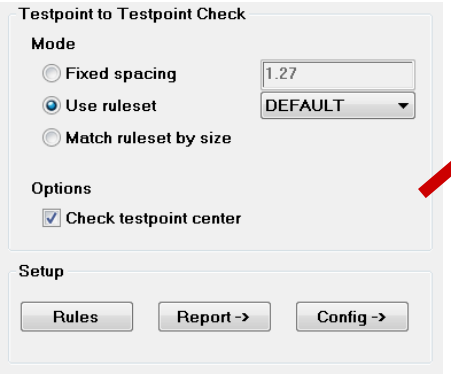


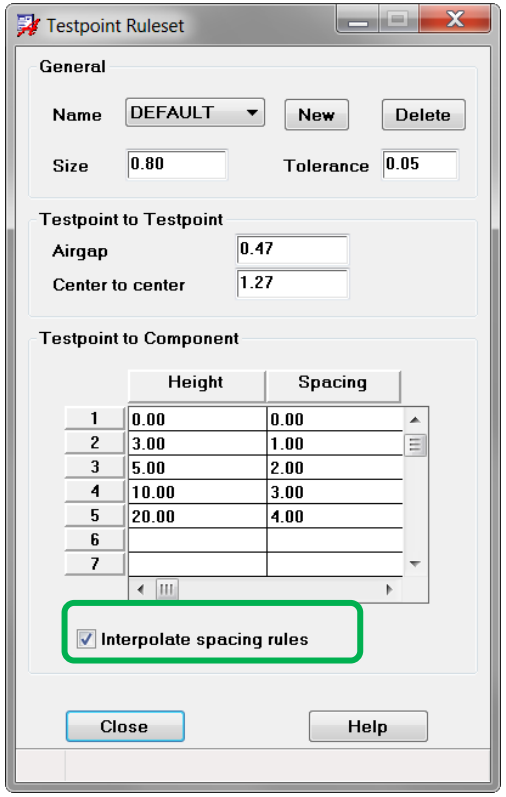


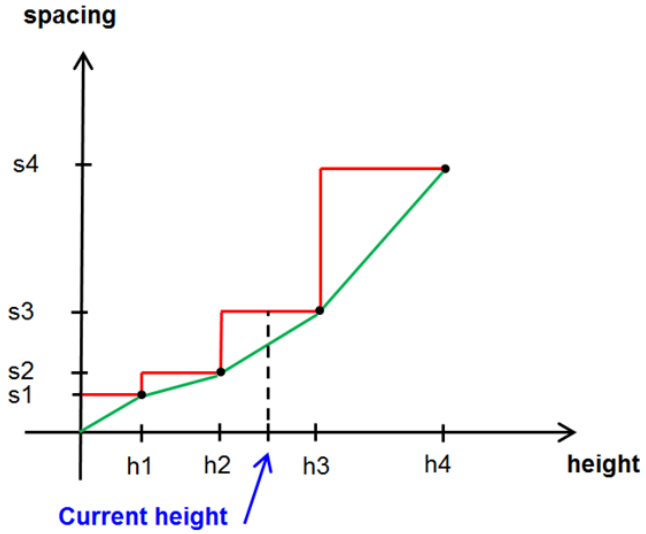
Advanced Testpoint Check

- Spacing rules may be specified
  - As fixed spacings
  - Using rulesets, which account for component height



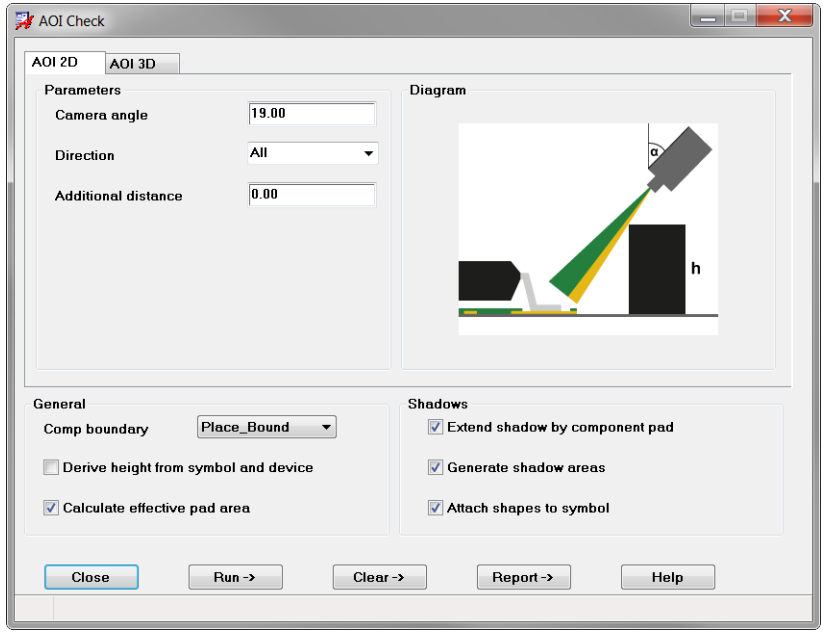


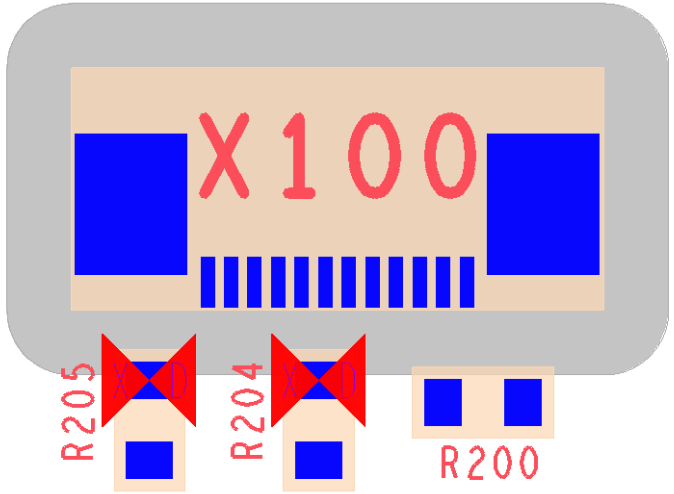


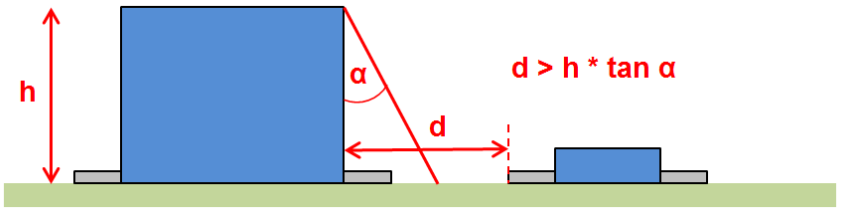


AOI Check

- Helps users to check AOI related rules directly in **PCB Editor**
- Shadowing can cause serious issues in verification process

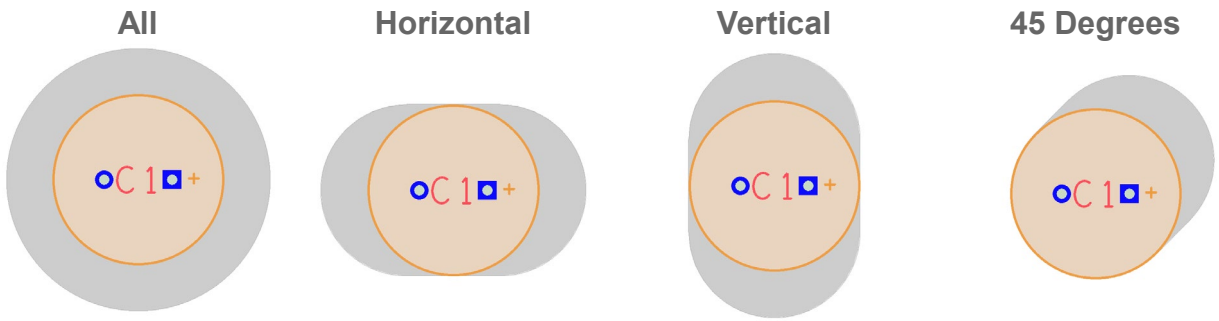




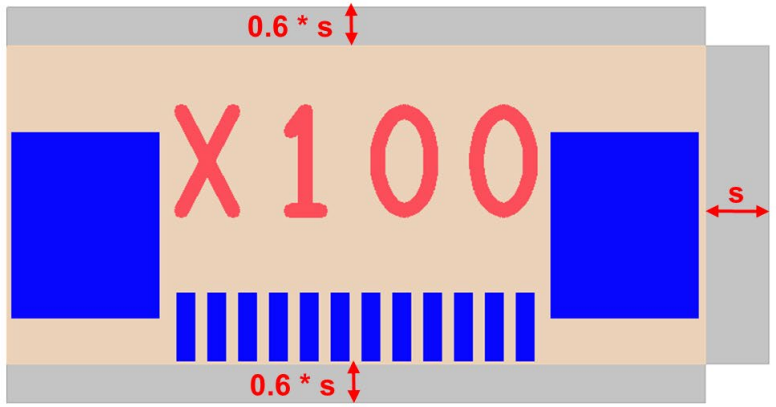


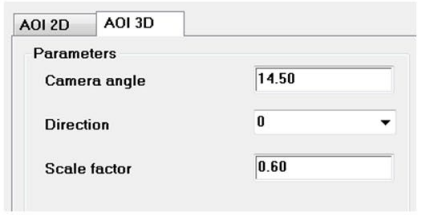
AOI Check

- Shadows can be calculated in various directions based on specified camera angles taking component height into account



- Special rules apply to 3D inspection systems

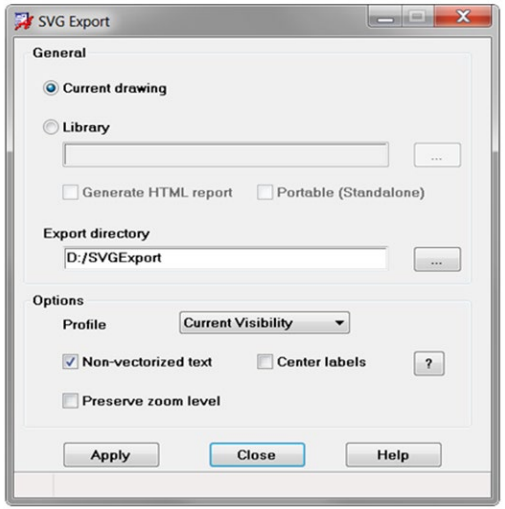


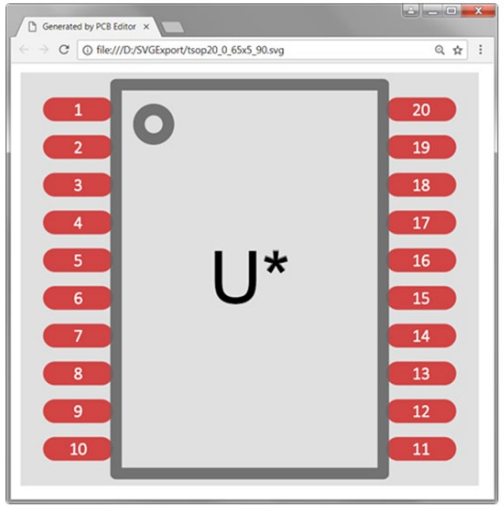


SMT flow direction

SVG Export

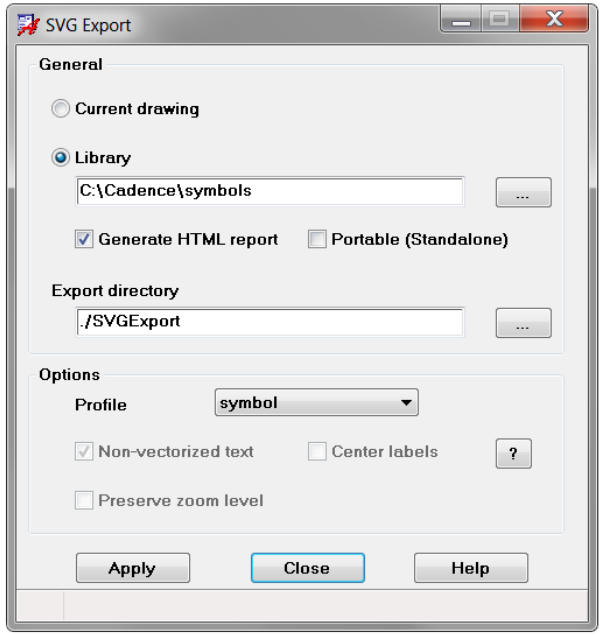
- Generates SVG data out of **PCB Editor**
- Export SVG from current drawing
- Export SVG's for a complete footprint library including HTM report generation
- Profile support
  - Content (layers) and styles (e.g. colors, opacity, non-vectorized texts, etc.) can be specified using predefined profiles

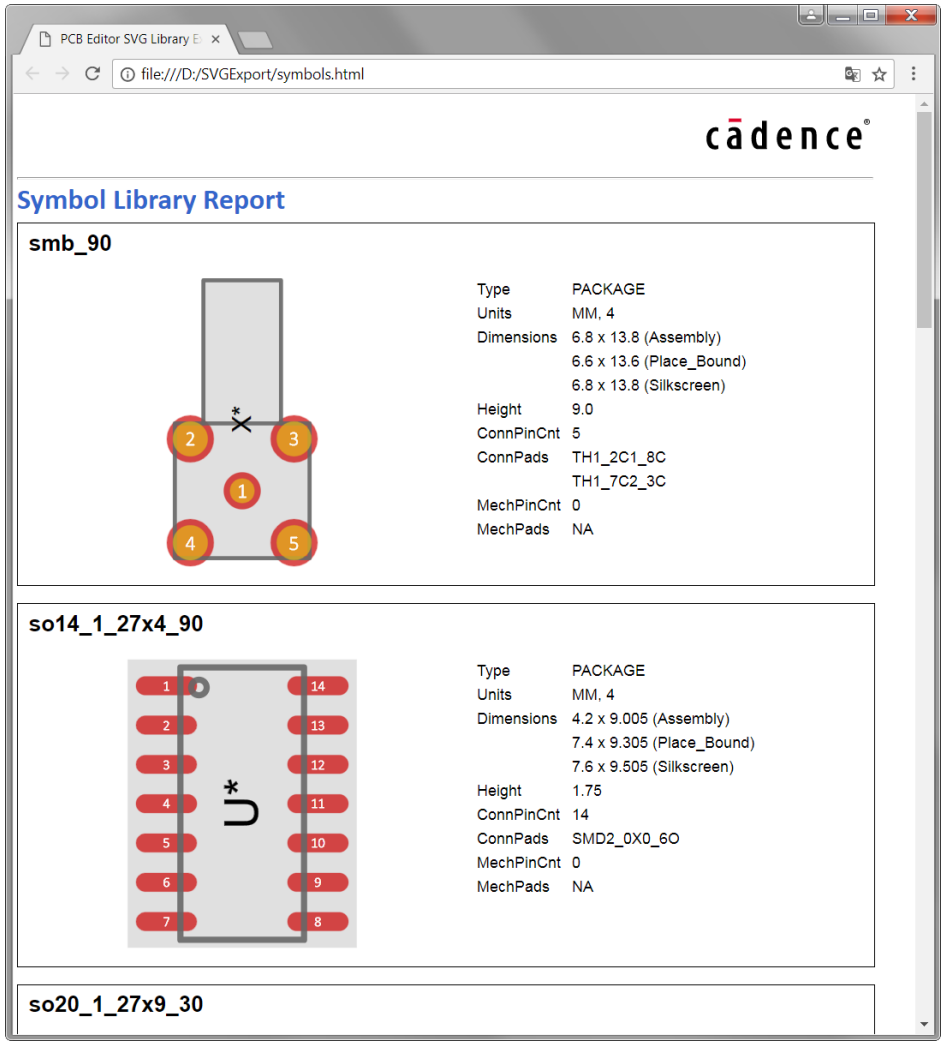




SVG Export

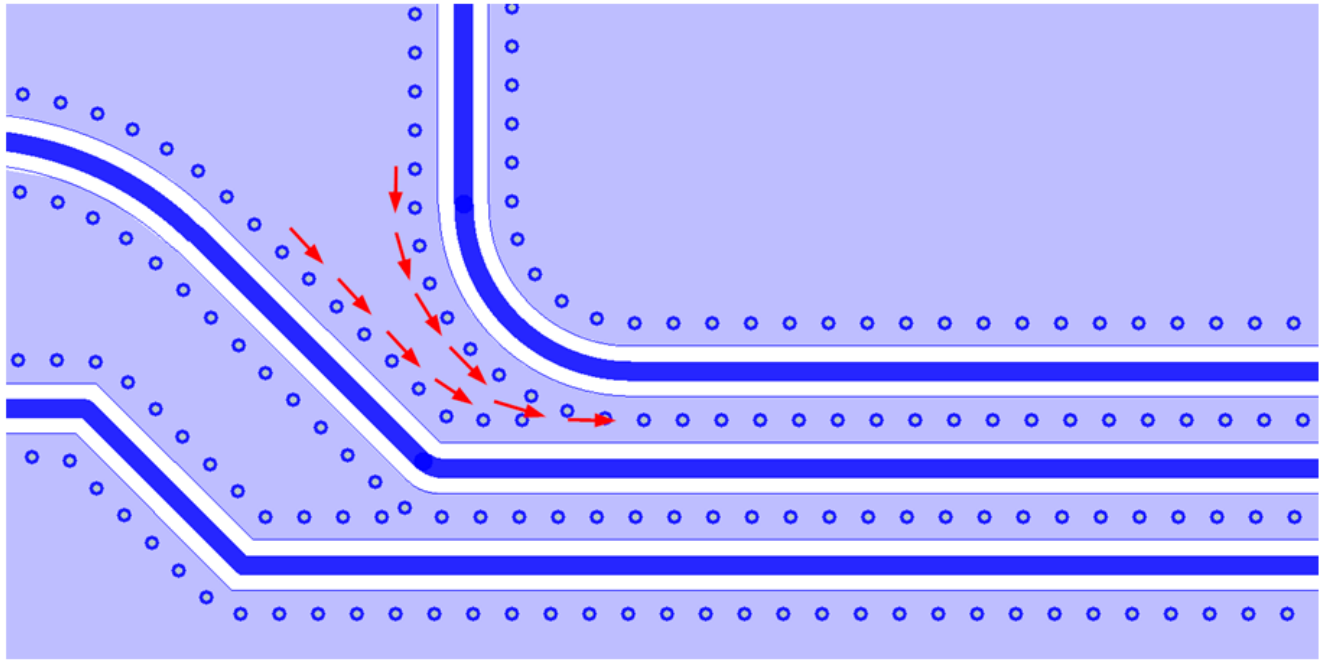
- Example for HTML library report





Shield Router Enhancement

- Support for via pattern sharing

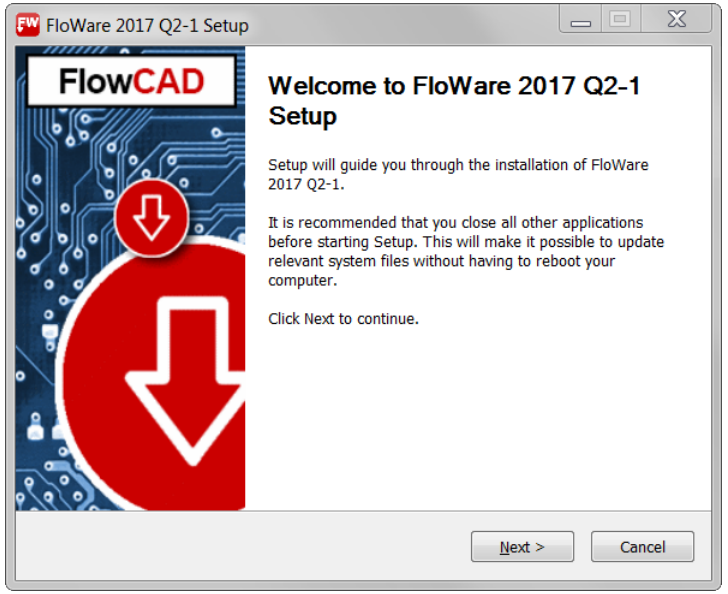


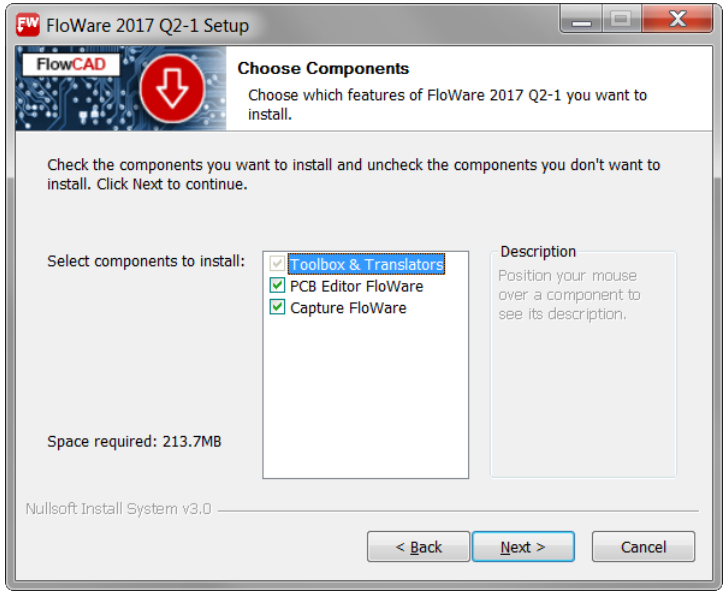
FloWare 2017

- **FloWare Installer**
  - New module
  - Executable which guides users through the installation
- **Silkscreen**
  - New module
  - Silkscreen generation including DRC check
- **Shield Generator**
  - New module
  - Generate ESD rings and shield boxes including via pattern
- **Padstack Usage**
  - New module
  - Library report utility

Installer Support

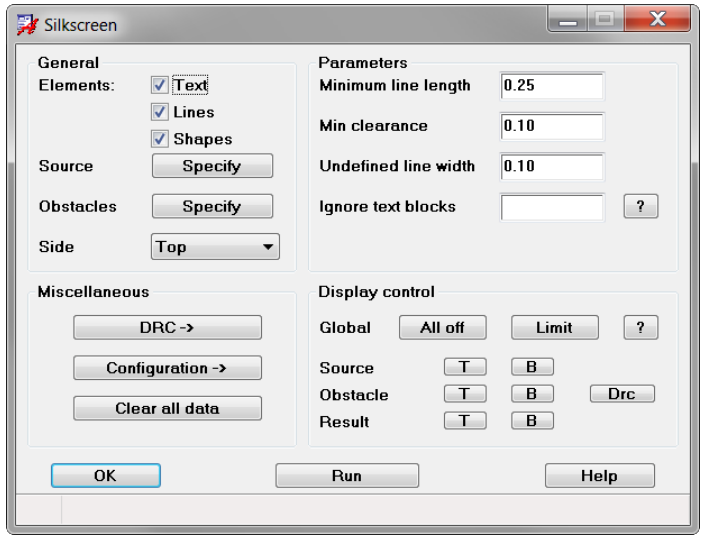
- Executable which guides users through the installation
- Toolbox & Translators
- PCB Editor FloWare
- Capture FloWare

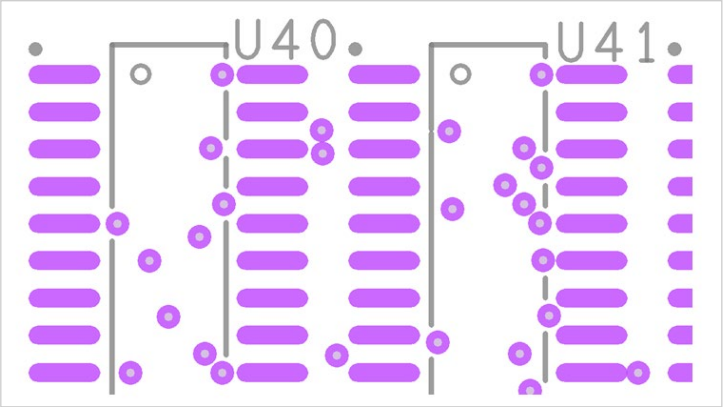


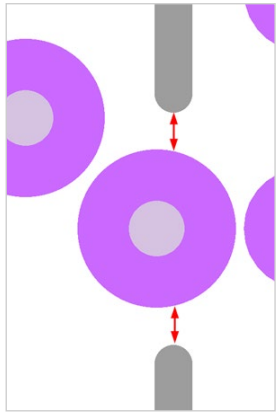


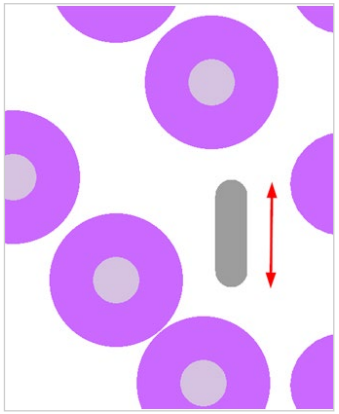
Silkscreen

- Powerful silkscreen utility
- Configuration
  Objects to silk e.g. lines and labels can be configured as well as obstacles which require silk objects to be cut e.g. soldermask, keepout areas
- Rules
  Clearances and minimum segment length can be defined



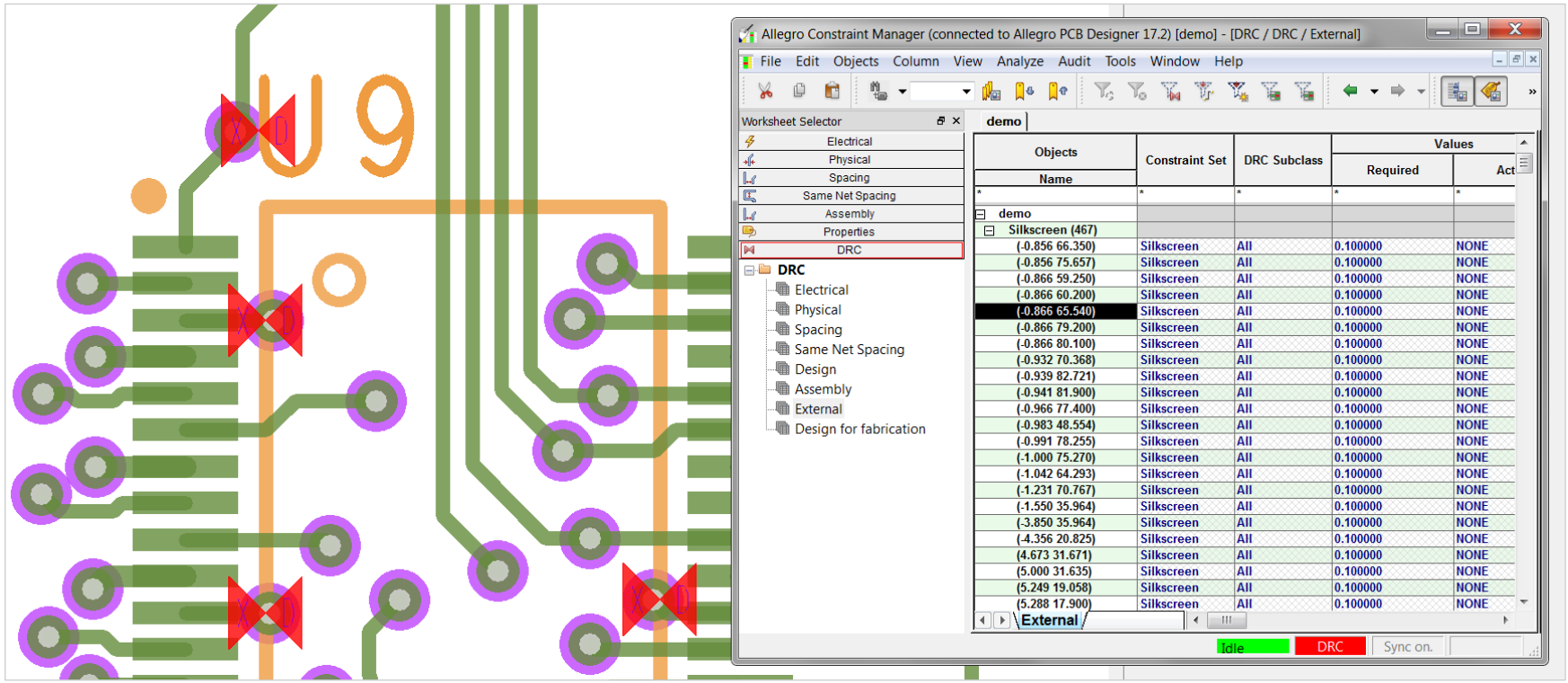






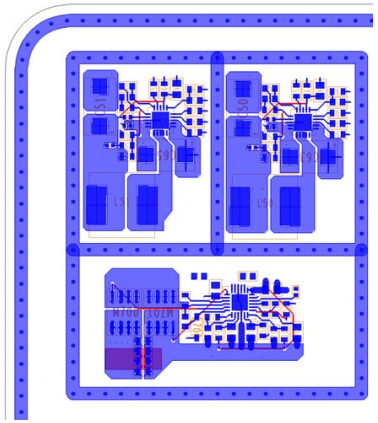
Silkscreen

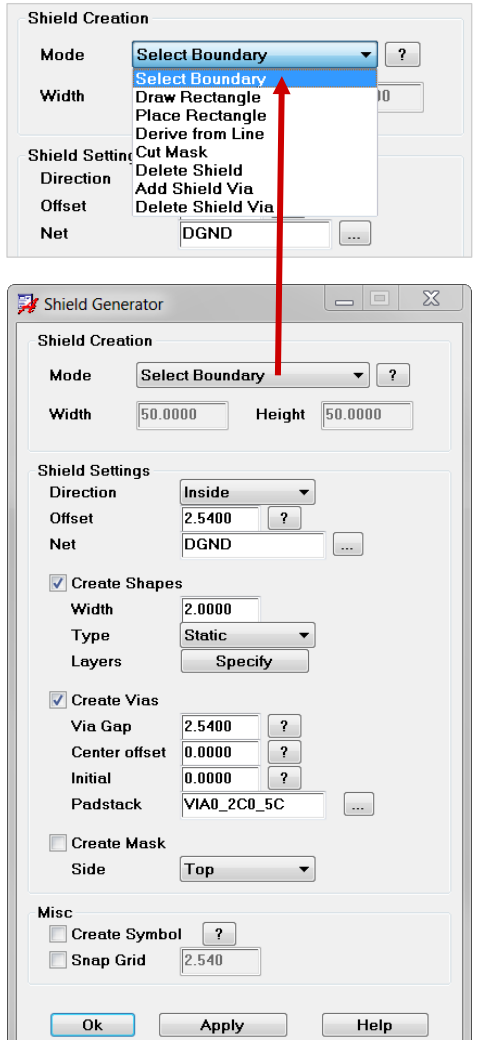
- DRC
  Before generating silkscreen data, a DRC check can be performed, indicating all violations helping users to identify problems and fix them before actual data is generated



Shield Generator

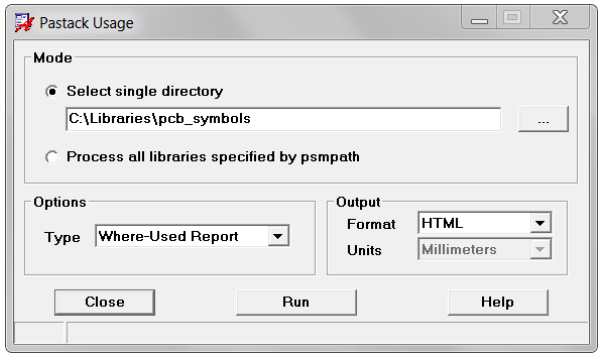
- Facilitates the generation of shape and via pattern for shielding purposes
  - ESD rings
  - Shield boxes for RF circuits
- Different modes for shield generation
  - Select Boundary
  - Draw / Place Rectangle
  - Derive from Line
- Shape parameters
- Via parameters
- Mask generation and cutting capabilities for solder mask and paste mask
- Ability to create groups or symbols

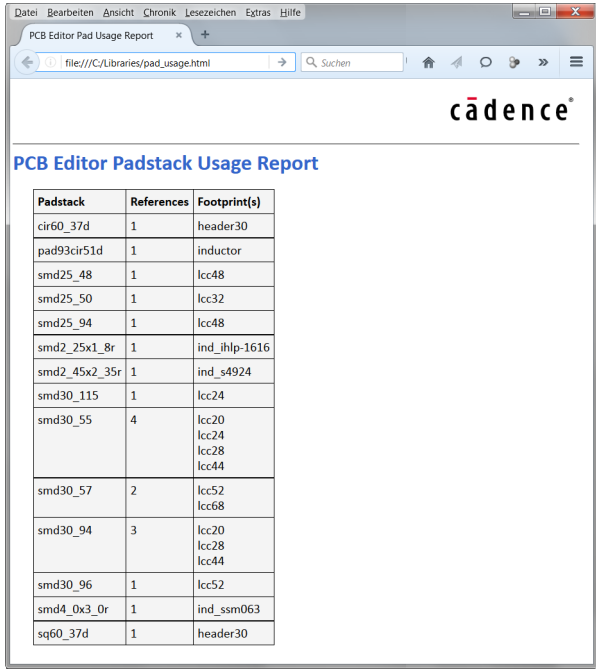




Padstack Usage

- Generate padstack reports by extracting data from PCB Editor symbol libraries (*.dra). Different reports are available
- Report types
  - Where-Used
    Lists all footprints that use a given padstack
  - Padstack Standard
    Lists the padstack definitions for a given footprint
  - Padstack Detailed
    Lists detailed information for a given footprint.
    This information includes number of pins, vias and mechanical pins, pin numbers, xy coordinates, etc.
- Report format
  - HTML
  - Excel
  - Text





Padstack	References	Footprint(s)
cir60_37d	1	header30
pad93cir51d	1	inductor
smd25_48	1	lcc48
smd25_50	1	lcc32
smd25_94	1	lcc48
smd2_25x1_8r	1	ind_ihlp-1616
smd2_45x2_35r	1	ind_s4924
smd30_115	1	lcc24
smd30_55	4	lcc20 lcc24 lcc28 lcc44
smd30_57	2	lcc52 lcc68
smd30_94	3	lcc20 lcc28 lcc44
smd30_96	1	lcc52
smd4_0x3_0r	1	ind_ssm063
sq60_37d	1	header30

Padstack Usage

Report Examples

Datei Bearbeiten Ansicht Chronik Lesezeichen Extras Hilfe

PCB Editor Pad Usage Report

file:///C:/Libraries/pad_usage.html

cādence

PCB Editor Padstack Usage Report

Padstack	References	Footprint(s)
cir60_37d	1	header30
pad93cir51d	1	inductor
smd25_48	1	lcc48
smd25_50	1	lcc32
smd25_94	1	lcc48
smd2_25x1_8r	1	ind_ihlp-1616
smd2_45x2_35r	1	ind_s4924
smd30_115	1	lcc24
smd30_55	4	lcc20 lcc24 lcc28 lcc44
smd30_57	2	lcc52 lcc68
smd30_94	3	lcc20 lcc28 lcc44
smd30_96	1	lcc52
smd4_0x3_0r	1	ind_ssm063
sq60_37d	1	header30

Datei Bearbeiten Ansicht Chronik Lesezeichen Extras Hilfe

PCB Editor Pad Usage Report

file:///C:/Libraries/pad_usage.html

PCB Editor Padstack Usage Report

Footprint	Definitions	Padstacks(s)
header30	2	cir60_37d sq60_37d
ind_ihlp-1616	1	smd2_25x1_8r
ind_s4924	1	smd2_45x2_35r
ind_ssm063	1	smd4_0x3_0r
inductor	1	pad93cir51d
lcc20	2	smd30_55 smd30_94
lcc24	2	smd30_115 smd30_55
lcc28	2	smd30_55 smd30_94
lcc32	1	smd25_50
lcc44	2	smd30_55 smd30_94
lcc48	2	smd25_48 smd25_94
lcc52	2	smd30_57 smd30_96
lcc68	1	smd30_57

Datei Bearbeiten Ansicht Chronik Lesezeichen Extras Hilfe

PCB Editor Pad Usage Report

file:///C:/Libraries/pad_usage.html

cādence

PCB Editor Padstack Usage Report

Footprint	Pins/Vias/Mech	Type	Number	Padstack	X	Y
header30	30/0/0	Pin	1	sq60_37d	0.000	0.000
		Pin	2	cir60_37d	2.540	0.000
		Pin	3	cir60_37d	5.080	0.000
		Pin	4	cir60_37d	7.620	0.000
		Pin	5	cir60_37d	10.160	0.000
		Pin	6	cir60_37d	12.700	0.000
		Pin	7	cir60_37d	15.240	0.000
		Pin	8	cir60_37d	17.780	0.000
		Pin	9	cir60_37d	20.320	0.000
		Pin	10	cir60_37d	22.860	0.000
		Pin	11	cir60_37d	25.400	0.000
		Pin	12	cir60_37d	27.940	0.000
		Pin	13	cir60_37d	30.480	0.000
		Pin	14	cir60_37d	33.020	0.000
		Pin	15	cir60_37d	35.560	0.000
		Pin	16	cir60_37d	0.000	-2.540
		Pin	17	cir60_37d	2.540	-2.540
		Pin	18	cir60_37d	5.080	-2.540
		Pin	19	cir60_37d	7.620	-2.540

pad_usage.xml - Microsoft Excel

	A	B	C
1	Padstack	References	Footprint(s)
2	cir60_37d	1	header30
3	pad93cir51d	1	inductor
4	smd25_48	1	lcc48
5	smd25_50	1	lcc32
6	smd25_94	1	lcc48
7	smd2_25x1_8r	1	ind_ihlp-1616
8	smd2_45x2_35r	1	ind_s4924
9	smd30_115	1	lcc24
10	smd30_55	4	lcc20
11			lcc24
12			lcc28
13			lcc44
14	smd30_57	2	lcc52
15			lcc68
16	smd30_94	3	lcc20
17			lcc28
18			lcc44
19	smd30_96	1	lcc52
20	smd4_0x3_0r	1	ind_ssm063
21	sq60_37d	1	header30
22			
23			

Padstack Usage Report

Contact us / Kontakt zu FlowCAD

Please do not hesitate to contact us.
Für weitere Fragen und Informationen stehen wir gerne zur Verfügung.

FlowCAD Deutschland
Mozartstr. 2
85622 Feldkirchen bei München
T +49 89 45637-770
info@FlowCAD.de

FlowCAD Schweiz
Hintermättlistr. 1
5506 Mägenwil
T +41 56 485 91 91
info@FlowCAD.ch

FlowCAD Polska
ul. Sąsiedzka 2A
80-298 Gdańsk
T +48 58 727 90 90
info@FlowCAD.pl

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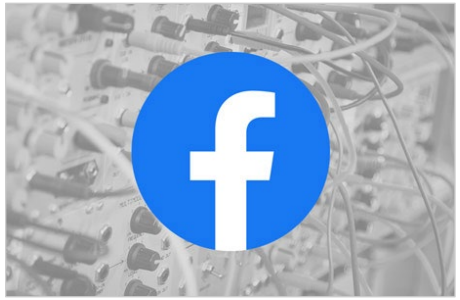

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